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Integration of innovative ohmic contacts for heterogeneous III/V-Silicon Photonic devices

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Thèse de doctorat de Physique

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Titre de la thèse :
Intégration de contacts innovants pour dispositifs photoniques III/V-Si

Résumé :
Depuis les années 2000, en raison d'une multitude de moyens de communication émergents, les besoins en termes d'échange de données n'ont cessé d'augmenter. Ces modifications ont conduit à l'initiation d'une transition depuis les technologies électroniques vers les technologies et interconnexions optiques. Entre autres, ces nouvelles technologies nécessitent l'utilisation de composants émetteurs et récepteurs de photons constitués de matériaux III-V. De façon à miniaturiser ces composants et à augmenter leurs performances tout en diminuant leur coût de fabrication, un modèle d'intégration innovant consiste à intégrer directement les sources III-V sur le circuit photonique silicium 200 mm. Afin d'optimiser les performances du laser III-V tout en respectant les contraintes liées à une salle blanche front-end / middle-end silicium, la réalisation d'une telle intégration nécessite notamment le développement de contacts innovants sur n-InP et p-InGaAs.
Ces travaux de thèse sont ainsi centrés autour du développement d'une nouvelle architecture de contacts répondant aux exigences d'une salle blanche front-end / middle-end silicium 200 mm, tout en optimisant les performances du laser III-V. Un schéma d'intégration innovant des contacts est tout d'abord présenté dans sa globalité puis une optimisation des procédés d'intégration disponibles est proposée. Ceci permet de profiter de l'avantage économique que procure le fait d'utiliser l'expertise existante tout en préservant les surfaces III-V et en optimisant les performances d'émission du laser. Une attention particulière est portée sur le développement de la métallisation de contact, elle-même reposant sur la formation de composés intermétalliques à l'interface entre le métal déposé et le semi-conducteur. Une étude métallurgique approfondie est ainsi conduite sur les systèmes Ni/n-InP, Ni/p-InGaAs et Ti/n-InP dans le but d'identifier les séquences de phases ainsi que des mécanismes mis en jeu et enfin leur stabilité thermique. Finalement, l'ensemble de ces métallisations sont intégrées au sein de dispositifs dédiés au test électriques des contacts. Les résistivités spécifiques de contacts associées sont ainsi extraites. Grâce à l'ensemble de ces travaux, les métallisations et procédés permettant d'optimiser les performances électriques des contacts intégrés tout en garantissant leur stabilité sont finalement identifiés.

Mots clefs :
Contact Métal/n-InP, Contact Métal/p-InGaAs, Photonique sur Silicium, Laser III-V, Intégration, Réaction à l'état solide, Caractérisation électrique, résistivité de contact.

Title:
Integration of innovative ohmic contacts for heterogeneous III-V/Silicon Photonic devices

Abstract:
Since the 2000s, the requirements in terms of data exchange never stopped rising owing to a multitude of emerging communication means. These extensive modifications lead the signal processing and electrical technologies to switch towards optical devices and interconnections. Among others, these new technologies require the use of III-V-based emitters and receptors. In order to miniaturize these devices, to optimize the performances and to minimize the fabrication cost of such a technology, an innovative manufacturing model consists in integrating directly the III-V laser source onto the 200 mm Si photonics circuit. To enable the development of contacts meeting the constraints of a front-end / middle-end Si-environment along with those of an operating laser, one of the keys lies in the development of contacts on n-InP and p-InGaAs which are necessary to electrically pump the III-V laser.
This Ph.D thesis therefore deals with the development of an innovative contact architecture fulfilling the requirements of a front-end / middle-end Si-dedicated clean room environment while optimizing the performances of the III-V laser. An integration scheme is firstly presented in its wholeness before optimizing every available process that is required. This kind of development leverages the advantage of utilizing existing infrastructures and processes while preserving the III-V surfaces and optimizing the performances of the III-V laser. Special attention is devoted to the development of the contact metallization which relies on the formation of intermetallic compounds at the interface between the deposited metal and the semiconductor. Extensive studies are therefore conducted on the Ni/n-InP, Ni/p-InGaAs et Ti/n-InP systems in order to identify the phase sequences, the involved mechanism and finally the thermal stability of the various phases. Ultimately, these metallizations are integrated in structures dedicated to their electrical characterization. The corresponding specific contact resistivities are thus extracted. Thanks to these studies, the metallizations and processes allowing an optimization of the electrical performances of the integrated contacts while ensuring their stability are finally identified.

Keywords:
Metal/n-InP contact, Metal/p-InGaAs contact, Si Photonics, III-V laser, Integration, Solid state reaction, Electrical characterization, Contact resistivity.

Nothing is impossible,

The word itself says 'I'm possible'!

[Audrey Hepburn]

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Lorsque je repense à ces trois années de thèse, de nombreux visages et échanges me viennent en tête. L'ensemble de ces travaux de thèse n'auraient pas été possibles sans l'investissement de nombreux acteurs. Je pense bien évidemment tout d'abord à ma directrice de thèse, Isabelle, sans qui cette thèse n'aurait pu aussi bien se dérouler. Je pense également à toutes les équipes du DTSI, qui, grâce à leur expertise et leurs conseils, nous ont permis de mener à bien l'intégration des contacts en salle blanche en quelques mois. Au-delà de ce travail quotidien, les interactions que j'ai pu avoir avec les différents experts ont également apporté une valeur ajoutée indéniable à ces travaux. Je pense également aux équipes du DCOS qui m'ont largement accompagnée au cours de ces trois ans. Je tiens notamment à remercier Yves dont les connaissances et l'aide nous ont permis de développer de nouveaux masques et d'imaginer une nouvelle intégration pour les contacts. Bernard et Claude ont également été d'une aide primordiale dans ces développements, que ce soit en termes de support au suivi de l'activité ou en termes de caractérisations, toujours en un temps record. Enfin, je souhaite remercier Louis pour les nombreuses discussions que nous avons eues autour des caractérisations électriques des contacts, mais aussi autour de sujets plus légers. L'ensemble de ces travaux de recherche a bien évidemment été mené en collaboration avec le département applicatif d'optoélectronique, le DOPT. En son sein, je souhaiterais tout d'abord remercier Bertrand pour son aide tout au long du projet. J'ai bien évidemment une pensée toute particulière pour Christophe qui n'a pas compté ses heures quand il s'agissait de m'expliquer les secrets de la photonique, ou de m'aider à intégrer les contacts. Dans ce cadre, je tiens également à remercier tout particulièrement Tiphaine et Jeremy pour leur efficacité et leur implication pour l'intégration des structures de test électriques.

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Un grand merci à vous tous ainsi qu'à tous ceux je j'aurais maladroitement oubliés.

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List of Acronyms

A

A	
AFM	Atomic Force Microscopy
AES	Auger Electron Spectroscopy
B	
BOX	Buried Oxide
BEOL	Back-End Of Line
C	
CMOS	Complementary Metal Oxide Semiconductor
CVD	Chemical Vapor Deposition
CMP	Chemical-Mechanical Polishing
CELO	Confined Epitaxial Lateral Growth

CTLM	Circular Transfer Length Method
D	
DIGS	Defect-Induced Gap States
DFB	Distributed Feedback Laser
E	
ESH	Environment Security Health
EDS /EDX	Energy-Dispersive X-Ray spectroscopy
F	
FIB	Focused Ion Beam
FEOL	Front-End Of Line
FFT	Fast Fourier Transform
FE	Field Emission
H	
HF	Hydrofluoric acid
HRTEM	High Resolution Transmission Electron Microscopy
I	
ITRS	International Technology Roadmap for Semiconductors
ICP	Inductively Coupled Plasma
L	
LASER	Light Amplification by Stimulated Emission of Radiation

M	
MQW	Multi Quantum Well
MEOL	Middle-End Of Line
MEMS	Micro-Electro-Mechanical Systems
MIGS	Metal Induced Gap States
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
P	
PIC	Photonic Integrated Circuit
PVD	Physical Vapor Deposition
PECVD	Plasma Enhanced Chemical Vapor Deposition
PDF	Powder Diffraction Files
R	
RTP / RTA	Rapid Thermal Processing / Annealing
RTA	Rapid Thermal Annealing
RMS	Root Mean Square
S	
SOI	Silicon On Insulator
SCH	Separate Confinement Heterostructure
SCL	Separate Confinement Layer

SEM	Scanning Electron Microscope
SBH	Schottky Barrier Height
SIMS	Secondary Ion Mass Spectrometry
SAD	Selected Area Diffraction
T	
TEOS	Tetraethyl orthosilicate (chemical formula: $Si(OC_2H_5)_{4)}$
TEM	Transmission Electron Microscopy
TOF	Time Of Flight
TLM	Transmission Line Model Transfert Length Method
TE	Thermionic Emission
TFE	Thermionic Field Emission
X	
XRR	X-Ray Reflectometry
XRD	X-Ray Diffraction
XPS	X-ray Photoelectron Spectroscopy

List of Symbols

Symbol	Signification	Units
A		
a	Length of the contact (TLM)	nm / µm
A*	Effective Richardson constant for thermionic emission	$A.cm^{-2}.K^{-2}$
A**	Effective reduced Richardson constant for thermionic emission	$A.cm^{-2}.K^{-2}$
D		
D_n	Diffusion coefficient for electrons	$cm^2.s^{-1}$
E		
e	Elementary charge	eV
E_0	Vacuum level energy	J
E_{00}	Characteristic energy for the determination of the dominant conduction mode	J
E_b	Schottky barrier height	J
E_C	Conduction band energy	J
E_F	Fermi level	J

E_{FM}	Metal Fermi level	J
E_{FSC}	Semiconductor Fermi level	J
E_g	Semiconductor bandgap	J / eV
E_V	Valence band energy	J
F		
h	Plank constant	J.s
$\hbar$	Reduced Plank constant	J.s
I		
I	Current	A
J		
J	Current density	$A.cm^{-2}$
$J_{M\rightarrow SC}$	Current density with a flux from metal to semiconductor	$A.cm^{-2}$
J_n	Electron flux current density	$A.cm^{-2}$
$J_{SC\rightarrow M}$	Current density with a flux from semiconductor to metal	$A.cm^{-2}$
J_{FE}	Reverse saturation current density in FE (field emission) conduction mode	$A.cm^{-2}$
J_{TE}	Reverse saturation current density in TE (thermionic emission) conduction mode	$A.cm^{-2}$
J_{TED}	Reverse saturation current density in thermionic emission diffusion theory	$A.cm^{-2}$
J_{TFE}	Reverse saturation current density in thermionic field emission diffusion theory	
J_D	Reverse saturation current density in diffusion theory	$A.cm^{-2}$
K		
k, k_B	Boltzmann constant	$J.K^{-1}$
L		
l_i	Spacing between two adjacent contacts (TLM)	m

L_T	Transfer lenght	nm / µm
	M	
m^*	Majority carriers effective mass	Kg
m_T^*	Majority carriers tunneling effective mass	Kg
	N	
N_A, N_a	Acceptor impurities concentration	$at.cm^{-3}$
N_C	Density of states in the conduction band	$at.cm^{-3}$
N_D, N_d	Donor impurities concentration	$at.cm^{-3}$
n(x)	Charge carriers concentration (electrons)	cm^{-3}
	O	
R_C	Contact resistance	Ω
R_E	End resistance	Ω
R_{SH}	Sheet resistance of the bulk semiconductor	$Ω / Ω.sq^{-1}$
R_{SK}	Sheet resistance of the semiconductor underneath the contact region	$Ω / Ω.sq^{-1}$
R_{sub}	Resistance of the substrate	Ω
R_{tot}	Total resistance measured	Ω
	T	
T	Absolute temperature	K
	V	
V	Voltage	V
V_a	Applied voltage	V
V_{bi}	Built-in voltage	V
V_F	Forward bias	V
V_R	Reverse bias	V

W		
W	Width of the contacts (TLM)	nm / µm
W_{dep}	Space charge region width	nm
X		
x_m	Distance from the metal / semiconductor interface of the extremum of potential energy	nm
γ		
γ	Sensibility of the Schottky barrier to the metal work function	-
δ		
δ	Interfacial layer thickness	Å
ΔΦ	Image-force barrier lowering	eV
ε		
E (chap II)	Electric field	$V.cm^{-1}$
ε_0	Permittivity of vacuum	$F.m^{-1}$
ε_s	Permittivity of semiconductor	$F.m^{-1}$
µ		
µ	Carrier mobility	$cm^2.V^{-1}.s^{-1}$
μ_n	Electron mobility	$cm^2.V^{-1}.s^{-1}$
ρ		
ρ_c	Specific contact resistivity	$\Omega.cm^2$
ϕ		
Φ_0	Charge neutrality level (relative to the valence band)	eV
Φ_b	Schottky barrier height	eV
Φ_{bn}	Effective Schottky barrier height for electrons	eV
Φ_{bp}	Effective Schottky barrier height for holes	eV
Φ_M	Metal work function	eV

Φ_n	Position of the Fermi level relative to E_C (n-type semiconductor)	eV
Φ_{SC}	Semiconductor work function	eV
	χ	
χ	Semiconductor affinity	eV
	ψ	
ψ_{bi}	Built in potential	eV

GENERAL INTRODUCTION

Since the 2000s, the requirements in terms of data exchange never stopped rising owing to a multitude of emerging communication means. These extensive modifications lead the signal processing and electrical technologies to switch towards optical devices and interconnections. Among others, these new technologies require the use of III-V-based emitters and receptors which are traditionally processed in III-V dedicated clean rooms on 2'' to 4'' wafers before being packaged in optoelectronic systems. In order to miniaturize these devices, to optimize the performances and to minimize the fabrication cost of such a technology, an innovative manufacturing model consists in integrating directly the III-V laser source onto the 200 mm Si photonics circuit. However, up to now these 200 mm wafers were reduced to 100 mm wafers after the bonding of the III-V laser and processed in III-V-dedicated clean rooms. In order to leverage the advantages of utilizing the silicon expertise and the existing Si-compatible equipments, an innovative integration is being developed by STMicroelectronics and the CEA-LETI in the frame of IRT Nanoelec Photonics programs. The latter consists in fully integrating the III-V laser on the 200 mm Silicon Photonics wafer and therefore in a 200 mm Si-compatible clean room after its bonding. In order to enable such an integration, one of the keys lies in the development of contacts on n-InP and p-InGaAs which are necessary to electrically pump the III-V laser. Because the contacts that were classically used on III-V lasers up to now are not compatible with a Si-compatible clean room in terms of integration and composition, a deep overhaul is required. The latter must enable the development of contacts meeting the constraints of a Si-environment along with those of an operating laser, *i.e.:*

- The contacts must be integrated on 200 or 300 millimeters-compatible equipments in a Si-compatible clean room thanks to planar processes which exclude any lift-off or related processes;
- All thermal budget must be minimized ($T \leq 450$ °C) in order not to degrade the active region of the laser composed of multi quantum wells;
- The materials in contact with / close to the active region of the laser must not generate important losses at the emitting wavelength of the laser;
- The contacts must be comprised of front-end compatible materials only, such as Ni, Ti and their alloys;
- The metallization must be selected to form ohmic contacts with specific contact resistivities lower than 5.10^{-5} Ω.cm².

Within this framework and in order to satisfy the above mentioned requirements, this Ph.D thesis was dedicated to the development of such innovative contacts.

After presenting the benefits offered by Silicon Photonics, Chapter 1 will present an overview of III-V / Si heterogeneous photonic integrated circuits. Several notions related to the integration and to the functioning of the III-V laser will be discussed in order to identify the critical parameters that could affect its functioning. The contacts that were classically integrated on III-V lasers in III-V dedicated clean rooms will then be presented in terms of composition and integration. This section will highlight the incompatibility of such contacts with 200 mm or 300 mm Si-compatible clean rooms, and therefore the need to develop innovative contacts.

Chapter 2 will thus be dedicated to the presentation of the innovative contacts' integration scheme that was fully developed in the 200 mm Si-compatible clean room. A special emphasis will be placed on optimizing the contacts while fulfilling the requirements of such an environment and without degrading the optical performances of the III-V laser.

After the overall presentation of the integration scheme, a particular attention will be paid to the contact metallization which must be chosen to form thermally stable and ohmic contacts both on n-InP and p-InGaAs. In order to develop fully Si-compatible contacts, the two metals that will be assessed are the Ni and the Ti. In chapter 3, the as deposited an annealed Ni/InP, Ni/InGaAs and Ti/InP systems will firstly be investigated thanks to metallurgical studies. The latter will enable an identification of the system's composition and morphology along with the related phase sequences and involved mechanisms.

Finally, chapter 4 will focus on the corresponding electrical study. After a description of the current transport mechanisms arising in a metal / semiconductor contacts, the Transfert Length Method (TLM), classically used to extract contact resistivities, will be presented and discussed. After these theoretical considerations, Si-compatible contacts presenting Ni and Ti-based metallizations will be electrically characterized thanks to dedicated test structures. Finally, in order to further optimize the electrical performances of these contacts, the effect of the dielectric encapsulation which is required in the frame of the innovative integration scheme will be probed.

To conclude, a scheme enabling the integration of the contacts on a III-V laser in a Si-compatible clean room will be displayed. The extensive studies conducted on the metallization will additionally enable the identification of the most adapted metal and subsequent thermal treatment on n-InP and p-InGaAs. Additional refinements will be proposed in order to further optimize the performances of the contacts and therefore of the overall laser device.

CHAPTER 1

INTRODUCTION TO SILICON PHOTONICS

Outline

1.1 The information revolution

Over the past decades the computing power of Complementary Metal Oxide Semiconductor (CMOS) based devices has considerably increased. While the dimensions of the transistors were scaled down, their integration density and switching speed never stopped rising. We have now reached a point where the calculation capacity is less limited by the performances of the devices than by the rate at which the data can be transferred. In this context, the electrical interconnects were identified as the upcoming bottleneck in the International Technology Roadmap for Semiconductors (ITRS) [1, 2]. It has become increasingly difficult for conventional metal based electrical interconnects to satisfy the design requirements in terms of power, bandwidth, delay and delay uncertainty. To address this issue, a transition from electrical to optical interconnects was proposed [1-5].

Optical interconnects offer various advantages ranging from wider bandwidths on longer distances and lower sizes to their insensibility to the electromagnetic noise. However, because of the cost advantage of their electrical counterparts, optical interconnects have usually ended up to be limited to long-distance links where the attenuation in copper cables is too high for the electrical circuits to compensate. Yet, their use becomes more and more required in the market of short distance links as they can meet the requirements in terms of data rates (Figure 1.1). To enable such a transition, optical technologies must be brought into the world of mass production.

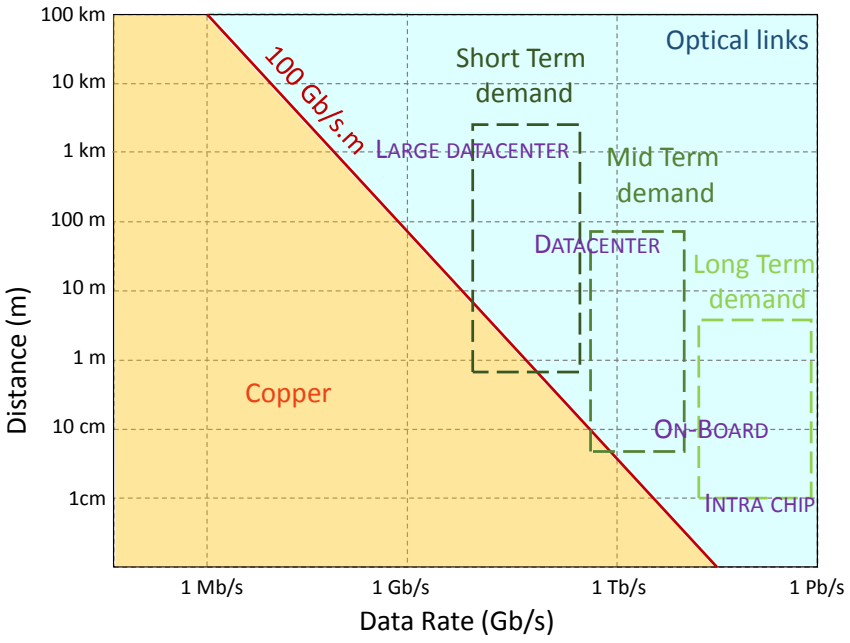


Figure 1.1 : Distance versus data rates of commercial electrical and optical interconnects. Electrical links are bounded by the 100 Gb/s-m bandwidth-distance product [6, 7].

1.2 Silicon photonics

1.2.1 Why do we need silicon photonics?

Following the path of miniaturization and integration in electronics, the concept of Photonic Integrated Circuit (PIC) emerged. The co-integration of several optical components on a chip opens the way to a miniaturization, a lowering of the manufacturing costs along with an increase of the complexity and performances of such devices. The integration of these optical components on Silicon wafers was firstly proposed by R. Soref during the 80s [8, 9] and leverages the economic advantages of utilizing existing infrastructures.

The important index contrast between silicon (n = 3.51) and its oxide (n = 1.45) makes Silicon On Insulator (SOI) a suitable platform for the integration of most photonics components (multiplexers, mirrors, resonant cavities…). Additionally, silicon being transparent at the wavelengths used for optical communication transmission (1.3 – 1.55 µm) SOI wafers are well adapted for optical guidance. Finally, this kind of wafers is widely used in microelectronics, abundant and available in large sizes (200 mm and 300 mm). The main issue lies in the fact that silicon cannot be used to produce the totality of the functions in a photonics circuit. While it is well adapted for the making of most active and passive components, its indirect band gap prevents it from being an efficient light emitter. In this respect, one solution is to heterogeneously co-integrate silicon with III-V materials[1] such as InGaAs, InP and InGaAsP. The latter are indeed widely used for the making of stand-alone emitting devices such as laser diodes because of their direct bandgap.

The meeting point between the worlds of Silicon and optics is that of Silicon Photonics. The current challenge is to identify and develop integration schemes on hybrid devices that would benefit from the silicon expertise and meet the requisites of the emerging photonics applications. In this thesis, a special attention will be paid to the development of CMOS-compatible contacts on III-V-based laser devices in this respect.

1.2.2 Description of a silicon photonics integrated circuit

In order to propagate the logical information from one hand of the device to the other, a silicon photonics circuit is made of several elementary components that we are briefly going to describe in the following section (Figure 1.2):

[1] III-V materials are composed of with at least one group III element and at least one group V element in the periodic table.

- A photon source, such as a semiconductor-based laser diode, emits light at a defined wavelength. One or several sources can be used in the case of a signal multiplexing. In this case, the several lasers must emit at different wavelengths that will give rise to different channels.
- A modulator converts the electrical information coming from the electronics circuit into an optical signal. An example of modulator is a Mach-Zehnder[2].
- A multiplexer is used to combine the several laser beams into one beam. The latter is separated into several channels (not shown in Figure 1.2).
- A waveguide or an optical fiber carries the optical signal to the other hand of the photonics circuit.
- A demultiplexer separates the various canals that where created by the multiplexer (not shown in Figure 1.2).
- Finally, a photo-detector converts the optical information into an electrical signal which will be processed in the CMOS circuit by the transistor afterwards.

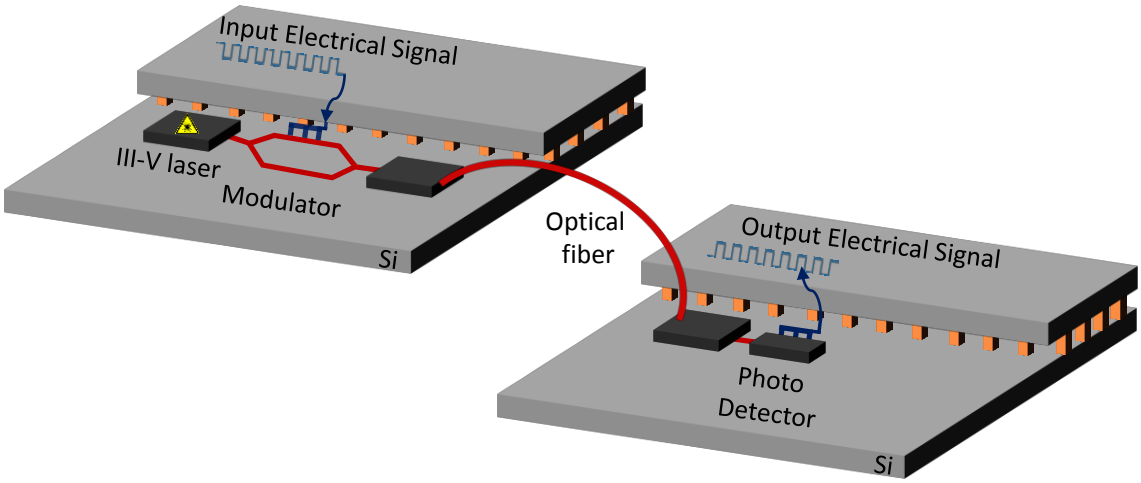


Figure 1.2 : Schematic representation of an optoelectronic circuit.

[2] In a Mach-Zehnder interferometer a beam splitter divides the laser light beam into two paths, one of which can be modulated in phase. The two beams are then recombined. Changing the electric field on the phase modulating path will then determine whether the two beams interfere constructively or destructively at the output, and thereby create logical 0 or 1.

1.3 III-V heterogeneous integration on Silicon

Several integration schemes can be used for co-integrating the III-V devices with the Si ones. In the following sections, we will discuss the most common techniques to achieve integration of III-V with silicon.

1.3.1 Hetero-epitaxial growth of III-V on silicon

Epitaxial growth of III-V materials on silicon might appear as the most fitted solution as it does not involve any alignment procedure which is critical between the laser and the entrance of the optical circuit. However, the lattice mismatch between silicon and III-V compounds is very important (8% between Si and Indium Phosphide (InP) or Gallium-Indium Arsenide ($In_{0.47}Ga_{0.53}As$, noted InGaAs in the following). Their thermal expansion coefficients are also very different from one another ($\alpha_{Si} = 2.6 \times 10^{-6}$ °C^{-1}, $\alpha_{InP} = 4.6 \times 10^{-6}$ °C^{-1}, $\alpha_{InGaAs} = 5.66 \times 10^{-6}$ °C^{-1}). Both characteristics result in an important density of defects (dislocations, phase boundaries…) which are severely harmful in active components as they act as non-radiative recombination sites[3]. A solution is to use buffer layers for example combining InGaP, low temperature grown GaAs, InP and a superlattice of InP/InGaAs [10]. While these layers allow a confinement of the defects, they are very thick (several micrometers) and therefore prevent an efficient evanescent coupling of the photons between the active device and the waveguide.

The CELO (Confined Epitaxial Lateral Growth) technique was proposed to overcome these issues [11]. High quality and defects free InGaAs and InP layers were grown on SiO_2 thanks to this method. Based on it, an integration scheme enabling an evanescent coupling between III-V layers and a silicon waveguide was demonstrated [12].

1.3.2 Flip Chipping

Flip chipping is a mature process that consists in reporting the individually fabricated III-V active device on top of the circuit. The interconnections are realized thanks to gold or gold-tin solder bumps. The main advantage of the solution is that the two elements being independently developed, they can be tested separately and the constraints linked to one do not affect the other. On the other hand, the important alignment precision required between the laser and the optical entrance of the circuit results in a slow and expensive alignment process. Moreover, the distance separating them

[3] Non-radiative recombination is a process in semiconductors whereby charge carriers recombine without releasing photons. A phonon is released instead. Non-radiative recombination in optoelectronics is an unwanted process as it lowers the light generation efficiency and increases heat losses.

typically corresponds to the thickness of the solder bumps, *i.e.*, a few micrometers, and further complicates the light coupling. Finally, the level of integration of such a technique is poor which results in a low compactness and in an increase of the fabrication costs.

1.3.3 Bonding of III-V on silicon

The last integration solution consists in bonding the III-V laser stack on a SOI wafer. The III-V carrier substrate is then removed in order to reveal the laser stack (Figure 1.3). An etching of the III-V is finally performed on top of the Si-based devices to form the T-shaped laser. As a consequence the laser alignment precision is that of lithography, meaning that it is only of a few tens to a few hundreds of nanometers. This integration method also provides a high crystalline quality leading to a good emitting efficiency of the laser. Three main bonding techniques are available:

- Metallic bonding

The metallic bonding is based on the use of a metallic alloy as a bonding agent. The most commonly used alloys are gold, tin and indium. The main advantage of this technique is that the bonding layer can also be used to dissipate a great part of the heat produced by the functioning devices. The main drawback is the important absorbency of such materials, leading to large losses in the case of evanescent coupling between the III-V laser and the waveguide located in the SOI wafer.

- Polymer bonding

The polymer bonding uses the DVS-BCB (divinylsiloxane benzocyclobutene) as a bonding via. The thickness of the BCB layer can be relatively small (down to 30 nm) and does not lead to any optical losses [13]. This bonding technique is particularly adapted to surfaces that present particles and/or roughness as both would be compensated by a deformation of the BCB.

- Direct bonding

The direct bonding utilizes the Van der Waals attraction that exists between two hydrophilic surfaces. To do so, an oxide layer (about 200 nm-thick) is either deposited on the substrates and planarized by chemical-mechanical planarization (CMP) or formed in an oxygen plasma. The two substrates are then put in contact at room temperature leading to the formation of Van der Waals bonds. A low temperature annealing process (T≈ 300 °C) converts these bonds into covalent ones. When using this technique, one can choose to bond III-V wafers (up to 150 mm [14]) or millimeters square dices to save the expensive III-V material. The main advantage of this technique compared to the polymer bonding is that oxide provides a better thermal conductivity than BCB (σ_{oxide} = 1.2

W/M.m ; σ_{BCB} = 0.3 W/M.m). This characteristic leads to a lower heating of the operating III-V laser and then to better emission characteristics. However, the direct bonding requires flat and defect-free surfaces (RMS roughness < 0.5 nm, bow < 10 µm and [defects] < 100 cm^{-2}). Because they share a high level of expertise in this field, the laser integration strategy followed by STMicroelectronics and the CEA-LETI exploits the direct bonding of III-V epitaxies on 200 mm SOI substrates.

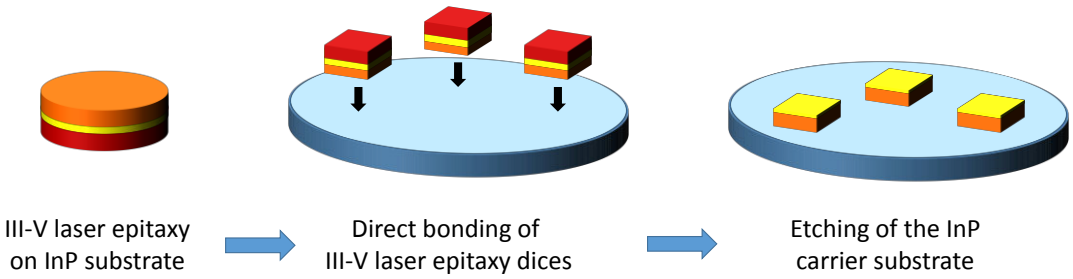


Figure 1.3 : Schematic representation of the direct bonding of III-V dices on Si substrates in the scope of Silicon Photonics.

1.4 The III-V laser structure

1.4.1 The LASER effect

While several types of laser exist (e.g., the hybrid evanescent lasers developed by UCSB and Intel [15] or the DFB lasers developed by the Tokyo Institute of Technology [16]) all of them are based on the same physical principal: the stimulated emission of photons. This principal has its origins in quantum physics and was described for the first time by Albert Einstein in 1917 [17]. The stimulated emission is related to another quantum phenomenon: the stimulated absorption of photons.

The stimulated absorption of photons occurs when a photon is sent on an atom. The absorption of this photon enables the transition of an electron to an upper energy level. The stimulated emission takes place when a photon is sent on this excited electron. The latter being disturbed by the incident photon, it goes back to its initial state releasing a second photon which is identical in all respects to the first one (Figure 1.4). As a consequence, the emitted photon has the same propagation direction, phase and polarity as the incident photon. The laser effect corresponds to the use of the cascaded stimulated emission phenomenon which gives rise to a coherent amplification of the signal and then to the LASER effect (Light Amplification by Stimulated Emission of Radiation).

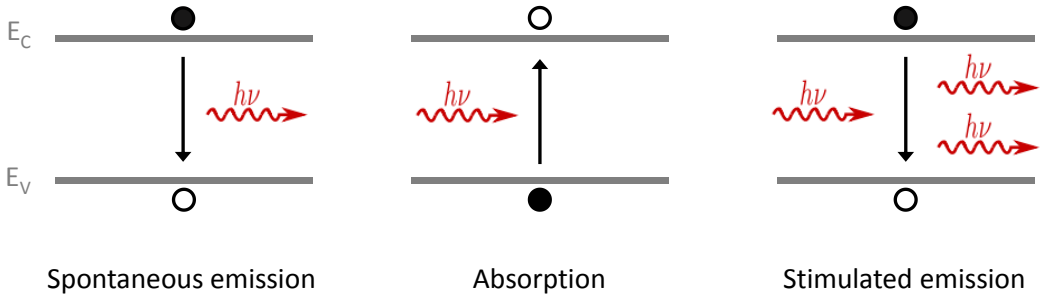


Figure 1.4 : Illustration of the electronic transitions that can occur between the conduction band and the valence band in a semiconductor. The stimulated emission of photons gives rise to a coherent amplification of the signal.

1.4.2 The laser structure

All lasers are composed of four basic building blocks as detailed in Figure 1.5: The *active region* is the zone where the stimulated emission of photons occurs. The latter relies on a population inversion that requires the supply of external energy provided by a *pumping system*. In order to maximize the probability of radiative recombination, the photons are forced to make round trips in the active region thanks to a *resonant cavity*. Finally, the created photons are extracted from the cavity and directed toward the waveguide by means of an *optic coupler*.

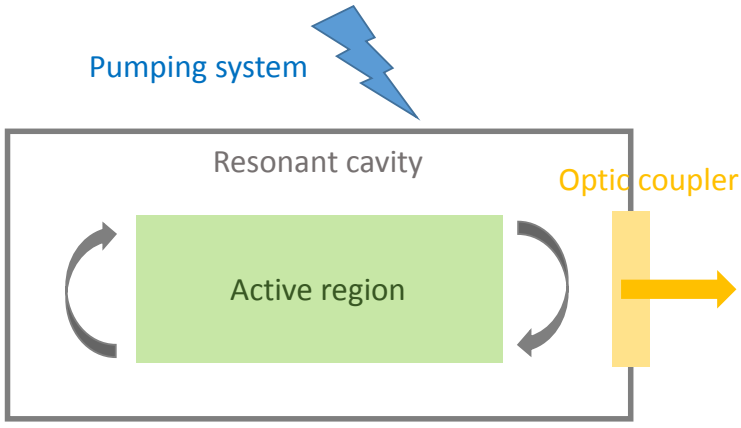


Figure 1.5: Schematic representation of the four elementary blocks constituting a laser: the active region, the resonant cavity, the pumping system and the optic coupler.

Active region and resonant cavity

The active region of the laser corresponding to the zone where the photons are created, it must be composed of semiconductors that present a direct band gap. The choice of the materials that compose this region is a function of the targeted emission wavelength. For example, InGaAsP and AlGaInAs are commonly used in the telecommunications where wavelengths range from 1.3 µm to 1.55 µm [18-24]. The amplification of the signal is maximized thanks to the use of quantum wells

which confine the charge carriers. The probability of radiative recombination and thus the gain at a given polarization are therefore increased. The thickness of the layers forming these quantum wells can be decreased down to the De Broglie electrons wavelength, *i.e.*, down to a few nanometers. The photons must also be confined so that they can make round trips in the active region, once again increasing the probability of stimulated emission. However, the wavelength of photons in the infrared being in the range of a few micrometers, their confinement cannot be achieved thanks to the quantum wells. This contradiction leads to the idea of a separate confinement heterostructure (SCH). Several thin layers form the quantum wells where the electrons and holes are trapped, while thick external layers, the separate confinement layers (SCL) guide the optical modes of photons [25] (Figure 1.6).

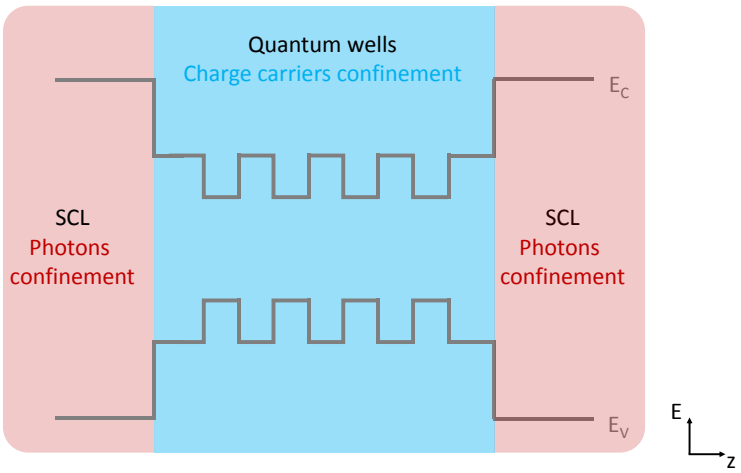


Figure 1.6: Typical band diagram (energy of conduction band E_C and valence band Ev versus growth direction) of quantum wells in separate confinement laser heterostructure (SCH).

Pumping system

In order to obtain a net production of photons in the active region, the stimulated emission process must dominate over the absorption. To do so, electrons must be promoted in the conduction band and holes in the valence band for a given *k*. This phenomenon called population inversion requires the use of degenerated semiconductors and the supply of external energy. The first requirement restricts the quasi Fermi levels positions into the valence (p-doped semiconductor) and conduction (n-doped semiconductor) bands and is described by the Bernard and Duraffourg inequality (Equation 1.1) [26].

$$e.V = E_{F,C} - E_{F,V} > h.\nu = E_g \qquad \textbf{Equation 1.1}$$

To meet the second requirement and supply the laser with energy, two main means are available: the optical and the electrical pumping. In the first case an external laser is used; its emitting energy must be higher than the band gap energy of the materials composing the active region. In this way, the atoms can be excited and emit photons when going back to their equilibrium state. When using the electrical pumping, the population inversion is achieved by integrating the quantum wells and SCH in a P-N junction. The polarization of the junction gives rise to the so called inversion zone. A subsequent voltage increase extends the width of this zone in the *k* space and increases as a consequence the radiative radiations as represented in Figure 1.7. We will see in the following sections that the lasers that we are dealing with in the frame of this PhD are electrically pumped, and therefore require the integration of innovative and efficient contacts.

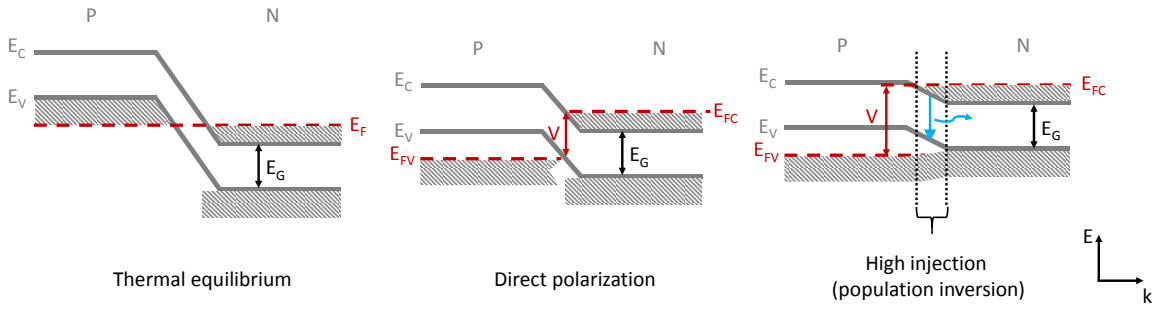


Figure 1.7: Schematic representation of the obtaining of the so called population inversion obtained thanks to a polarized P-N junction.

Resulting laser structure

When combining these elementary components, the resulting laser structure is composed of an InP-based P-N junction in which the multi quantum wells and SCL are placed. In STMicroelectronics and CEA-LETI's devices, this active region is composed of $InGa_xAs_{1-x}P_y$ layers emitting between 1.3 and 1.55 µm. Metallic contacts are integrated on each side of the P-N junction in order to electrically pump it. In this respect and to favor the formation of ohmic contacts ($\Phi_M > \Phi_{SC}$, where Φ_M and Φ_{SC} are respectively the work function of the metal and of the p-doped semiconductor), an additional p-InGaAs layer is epitaxially grown on top of the p-InP ($\Phi_{p\text{-}InP}$ = 5.65 eV and $\Phi_{p\text{-}InGaAs}$ = 5.29 eV). Finally, an InP/InGaAsP super lattice and an InP layer are added at the base of the laser to facilitate the bonding process. The arising laser structure is schematized in Figure 1.8.

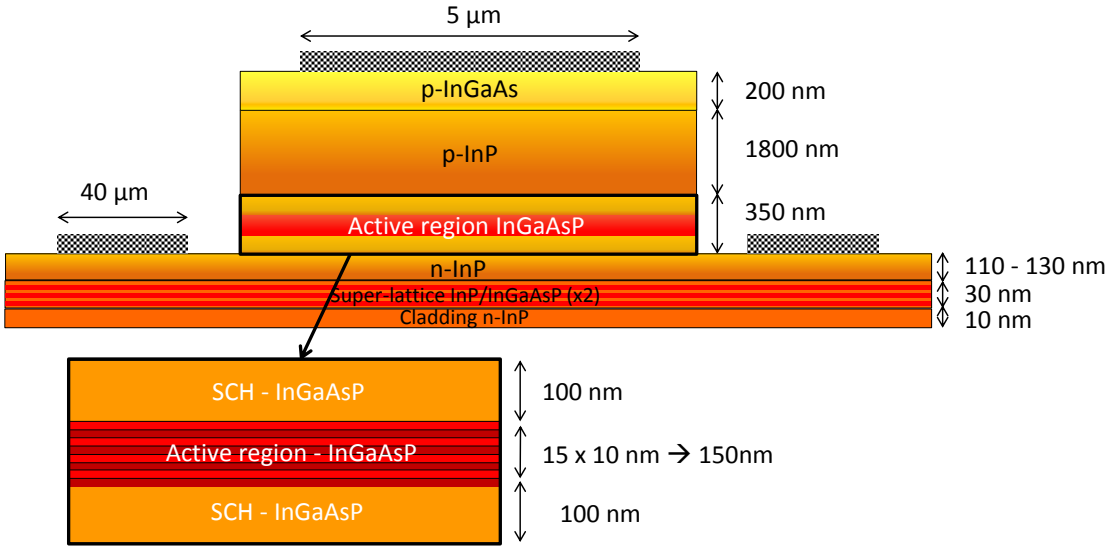


Figure 1.8: InP/InGaAsP-based laser structure used in STMicroelectronics and in the CEA-LETI. Note that the laser length is about 500 µm.

Optic coupler

Once the photons have been created in the III-V laser, an optic coupler must be used in order to couple the modes from the active region to the waveguide located in the SOI region. To do so, three options are available, keeping in mind that the optic modes are guided by the highest refraction index layers and that this parameter increases rapidly with the width of the waveguide before stabilizing [27].

- III-V guided mode

The first strategy consists in utilizing a III-V waveguide which presents a high effective index (index seen by the modes if the wave moved along a straight line in the waveguide) compared to that of Si. In this way, the fundamental mode is guided by the III-V and only the evanescent queue is located in the Si waveguide as represented in Figure 1.9a. The main advantage of this structure is that the gain is optimal but the coupling is weak.

- Si-guided mode

Contrary to the first solution, in this case the Si waveguide's index is higher than that of the III-V. The mode is then guided by the Si and only its evanescent queue is located in the III-V region (Figure 1.9b). As a result, the coupling of this kind of structure is optimized at the expense of the gain. When choosing this option, the thickness of the bonding layer must be minimized ($t < 100$ nm) as the mode overlapping exponentially decays with the distance between the two waveguides.

- Optic coupling between the III-V and the SOI

The third option consists in adiabatically coupling the optical mode between the III-V and the Si. To do so, the effective refractive index of the III-V and the Si are modified thanks to a taper which is a waveguide, here in the Si, composed of three different widths (Figure 1.9c). The effective refractive index decreasing rapidly when narrowing the waveguide, such a design allows converting gradually the first-waveguide mode into the second and reciprocally [28]. As a consequence such a structure is composed of a gain zone where the mode is confined in the III-V (thin Si guide), of a coupling zone allowing the transfer of the mode from the III-V to the Si (width of the Si guide that increases progressively), and finally of a passive zone where the mode is guided by the Si (wide Si region). In this way, both gain and coupling are optimized. Because this option allows an optimization of both the gain and the coupling, it was retained by STMicroelectronics and the CEA-LETI.

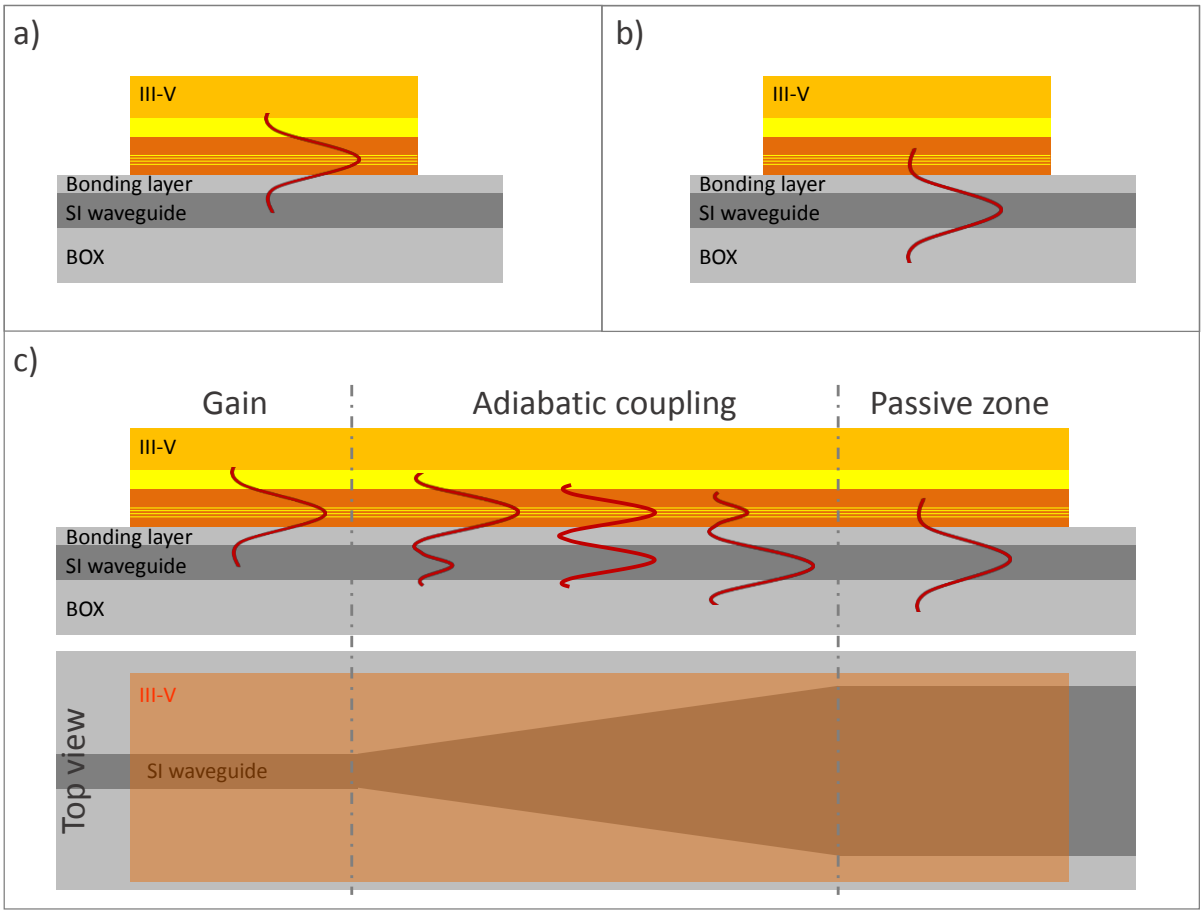


Figure 1.9: Modes coupling between the III-V and the Si waveguides. (a) III-V guided mode, (b) Si guided mode and (c) adiabatic coupling between the III-V and the Si.

1.5 The optical gain and losses

In a laser, stimulated emission and absorption are competitive phenomena. When electrically pumped, the laser needs to be under a sufficient polarization to obtain a net production of photons. However, other aspects have to be taken into account when designing this device to maximize the gain and minimize the photon losses.

1.5.1 The optical gain

The optical gain of a semiconductor laser defines the light amplification rate per unit length and is therefore expressed in cm^{-1}. It is positive when the stimulated emission of photons compensates their absorption. In other words, the optical gain is a function of the electronic transitions that occur between the conduction band and the valence band in the semiconductor. As described in section 1.4.1 and 1.4.2, the net production of photons can be obtained thanks to a polarized P-N junction in which the active region and resonant cavity are placed.

In the resonant cavity, the photons make round trips, and during this journey, some will be produced while others will be absorbed. The laser effect appears when the losses are exactly compensated by the gain, that is when the intensity after a round trip is equal to the initial one as indicated in Equation 1.2.

$$I_0 \text{ x } \exp(\text{gL}) \,.\, \exp(-\alpha\text{L}) \text{ x } R_1 \text{ x } \exp(\text{gL}) \,.\, \exp(-\alpha\text{L}) \text{ x } \text{R}_2 = \text{I}_0 \qquad \textbf{Equation 1.2}$$

With g the optical gain (cm^{-1}). This gain takes into account the intrinsic material gain and the confinement factor;

α the absorption coefficient;

R_1 and R_2 the reflection coefficient of the mirrors forming the resonant cavity;

L the length of the resonant cavity.

Equation 1.2 leads to the lasing threshold equation which defines the minimal gain which is necessary to initiate the LASER effect.

$$g_0 = \alpha + \frac{1}{2L} . ln\left(\frac{1}{R_1 R_2}\right) \qquad \textbf{Equation 1.3}$$

Threshold gain coefficients for InGaAsP/InGaAs or InGaAs/GaAs quantum well structures are typically of 500 cm^{-1} while the corresponding maximum material gain coefficients range from 3 x 10^3 to 6 x 10^3 cm^{-1} [29], [30], [31].

1.5.2 The optical losses

The optical losses correspond to the attenuation of the wave amplitude throughout its propagation and are therefore expressed in cm^{-1}. Generally speaking, these losses can be caused by internal absorptions in the waveguide materials or by external factors such as roughness induced scattering for example. In the following, we will discuss the main loss causes in the laser device that we will be dealing with throughout this thesis, such as represented in Figure 1.10.

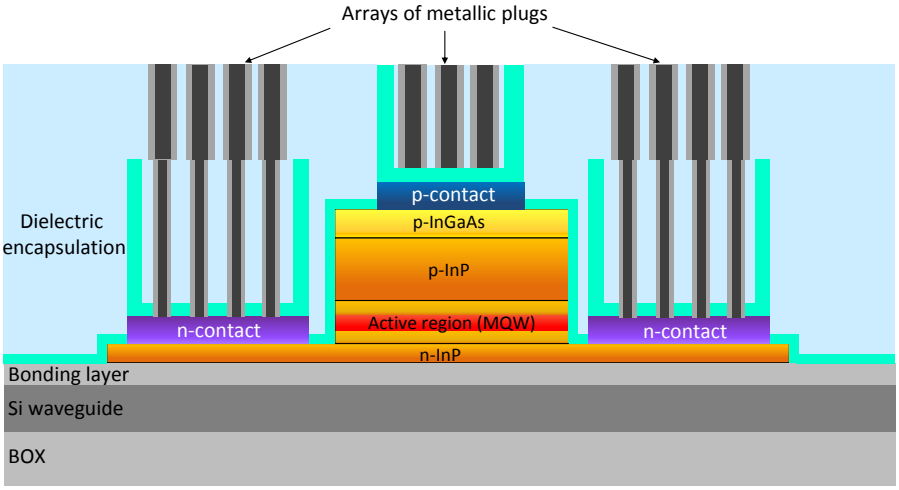


Figure 1.10: Schematic representation of a laser device with integrated contacts.

Internal absorption loss

In a direct band semiconductor several charge carriers' transitions lead to the absorption of photons (Figure 1.11) [31]:

- The Direct Band to Band (DBB) and Indirect Band to Band (IBB) absorptions;
- The Intra Conduction Band Valley absorptions (ICV);
- The Intra Conduction Band (ICB) absorptions corresponding to the transition of an electron from the bottom to the top of the conduction band;
- The Inter Valence Band (IVB) absorptions which correspond to the transition of a hole from a lower valence band to a higher one.

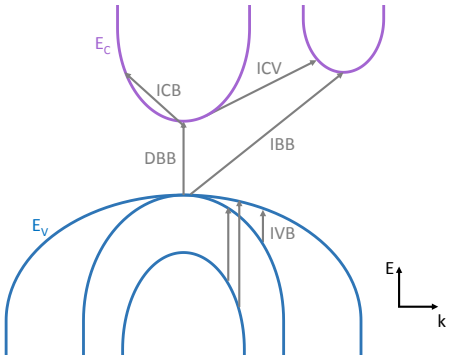


Figure 1.11: Intra and Inter band transitions in a direct band gap semiconductor leading to internal absorption losses.

The intensity of these mechanisms strongly depends on the wavelength. For $\lambda < \lambda_{Eg}$, the DBB and IBB transitions are favored while they exponentially decay for higher wavelengths. In this case, the absorption phenomenon is dominated by the free carriers induced losses (ICB, IVB and ICV). The corresponding absorption coefficient can be approximated by a linear function of the carriers' concentration:

$$\alpha_p = k_n.n + k_p.p \qquad \textbf{Equation 1.4}$$

Where n and p are the electrons and hole concentration and k_n and k_p the corresponding absorption coefficients.

The holes' absorption is particularly important in the InP, GaAs and InGaAs-based devices operating at the telecommunication wavelengths (1.3 - 1.55 µm) [31]. In these cases, the energy difference between the valence bands corresponds to the photon energy resulting in high α coefficients ranging from 13 cm^{-1} to 25 cm^{-1} for these three materials [32]. The intra conduction band transitions are responsible for a less important absorption in these materials (α = 1.5 cm^{-1} in InGaAsP/InP waveguides [33, 34]). The absorption induced by the p-type layers is then much more important than the one induced by n-type layers. Thus, it seems reasonable to evaluate the feasibility of an innovating integration where p-type layers would be replaced by n-type ones. In this respect designs integrating tunnel junctions coupled to n-type layers were proposed and allowed to reduce by half the generated losses in a 500 nm thick laser epitaxy [35].

Scattering loss

When propagating in a waveguide, light can suffer from losses caused by the defects it encounters. For example microscopic variations in the material density, compositional fluctuations, structural inhomogeneity and manufacturing defects can lead to important scattering losses. The latter can also be induced by the roughness the photons might encounter on the sidewalls of the waveguide. As a consequence, the manufacturing of the SOI waveguide is crucial to minimize the scattering losses.

Similarly, the etching of the III-V laser requires special attention in order to minimize the sides' roughness and the resulting losses.

Metal and dielectric absorption loss

Aside from the losses generated in the materials where the light propagates, some might be caused by the surrounding materials. Generally speaking the absorption of a material is described by the imaginary part of its complex refractive index: $N = n + ik$. When k is positive, the material is absorbent; when k is equal to zero, the material is transparent; when k is negative, the material is amplifier. As a result, the absorption coefficient of a given material can be calculated directly based on the imaginary part of its complex refractive index:

$$\alpha_p = \frac{4\pi k}{\lambda} \qquad \textbf{Equation 1.5}$$

The table below lists the real and imaginary parts of the refractive index of the most commonly used metals as contacts on both InP and InGaAs as well as the corresponding absorption coefficients at λ = 1.5 µm.

Table 1.1: Real and imaginary parts of the refractive index of the most commonly used metals as contacts on both InP and InGaAs along with the corresponding absorption coefficients at λ = 1.5 µm [36-38]

	Ti	Au	Ni	Pd	Pt
n	3.68	0.36	3.49	2.91	5.31
k	4.54	10.40	7.02	8.15	7.04
α (cm^{-1})	3.8×10^5	8.7×10^5	5.9×10^5	6.8×10^5	5.7×10^5

The listed absorption coefficients are on average two orders of magnitude greater than the material gain coefficient of a 6 quantum-wells-InGaAsP based diode [29]. For this reason metallic contacts must be placed as far away as possible from the active region of the laser and from the waveguides. The lower contacts being placed aside from the active region, their influence is negligible. However, the influence of the upper contact can be important in case of thin epitaxies as the optical mode intensity is mainly located underneath the contact. In this case, the use of contacts located on the top edges is a promising solution.

As represented in Figure 1.10 and detailed in Chapter 2, the CMOS-compatible integration of the contacts is enabled by a dielectric encapsulation of the laser. Just like metallic contacts, these

dielectric compounds can generate absorption losses because of their vicinity from the active region of the laser. As taking them away from the quantum wells is not possible, section 2.4 will be dedicated to their optical characterization and selection.

Radiation loss

Aside from the absorption loss, the dielectric compounds can be responsible for the so called radiation loss. More precisely, in this case, the refractive index difference between these materials and the III-V generate losses. The latter appear when a material with a higher refractive index than that of the region where the optical modes are located is placed next to it. Let's consider for example a 300 nm thick waveguide composed of InP (n = 3.16 @ 1.3 - 1.55 µm) bonded to a Si substrate (n = 3.5 @ 1.3 - 1.55 µm) thanks to a SiO_2 layer (n = 1.44 @ @ 1.3 - 1.55 µm). Non negligible losses are generated by the vicinity of the Si from the InP waveguide. It was demonstrated that a SiO_2 bonding layer thickness of at least 550 nm is necessary to minimize these losses down to 1 cm^{-1} [35].

1.6 The electrical pumping of the laser: contacts to n-InP and p-InGaAs

1.6.1 State of the art about contacts to III-V materials

In order to enhance the performances of the laser, the above detailed losses must be minimized while the gain must be maximized for a given polarization. Because the laser devices that are used by STMicroelectronics are electrically pumped, one of the most important developments therefore concerns the contacts that are integrated on each side of the P-N junction. Indeed, as explained in section 1.4.2, the polarization of the junction determines the width of the inversion zone, and therefore the intensity of the radiative radiations.

As a consequence, just like electronics, photonics require the use of high quality contacts to provide both short and long term performances and reliability. In this respect, contacts to III-V surfaces have been developed over the past decades taking into account several expectations as listed below whatever the targeted application. Note that these contacts will be referred to as *classical contacts* in the following, as opposed to the Si-compatible *innovative contacts* whose development is the heart of the present thesis.

- The metallization must be selected to form ohmic contacts (see Chapter 4 for a detailed definition) and must present the lowest sheet resistance, therefore limiting their contribution to the overall resistance;

- The deposition temperature and the subsequent annealing treatments must be carefully chosen to form interfacial products that lower the contact resistivity while limiting the induced stress;
- The compounds along with their microstructure must be stable over a large range of processing temperatures;
- The number of lithography in the integration scheme must be minimized in order to lower the overall production cost.

To this end contacts to III-V surfaces have been extensively studied over the past decades. Generally speaking, classical contacts to n-InP and p-InGaAs are comprised of a multitude of layers which were added over the years to address encountered issues or to push back the limits in terms of specific contact resistivity lowering. In the following, we provide non-exhaustive lists of the classical stacks, annealing treatment conditions, III-V doping level and resulting specific contact resistivity both on n-InP (Table 1.2) and p-InGaAs (Table 1.3). Note that the nomenclature convention that will be used throughout this chapter is as follows: the contacts' stacks will be noted A/B/C, where C is the layer in contact with the semiconductor.

Classical contacts to n-InP

Table 1.2: Classical contacts stacks, annealing treatment conditions, III-V doping level and resulting specific contact resistivity on n-InP surfaces

Metallization	Annealing treatment	InP doping level [cm^{-3}]	ρ_c [$\Omega.cm^2$]	Reference
AuGe	480 °C – 90 s	1×10^{18}	4.0×10^{-7}	[39]
Ni/AuGe	440 °C or 480 °C - 90 s	1×10^{18}	1.3×10^{-7}	[39]
Pd/Ge	300 °C – 30 min	5.3×10^{18}	1.3×10^{-5}	[40]
Pd	300 to 350 °C – 2 min	1.8×10^{18}	5.0×10^{-7}	[41]
Au/Ge/Pd	350 °C – 320 s	1×10^{17}	2.5×10^{-6}	[42]
Al/W/Pd/Ge/Pd	450 °C – 30 s	3×10^{18}	7.2×10^{-8}	[43]
Ge/Pd	400 to 450 °C - < 10 min	1×10^{17}	4.2×10^{-6}	[42]
Ge/Pt	450 °C – 10 min	2×10^{18}	2.0×10^{-5}	[44]
Ge/Pt/Ge/Pt	500 °C – 30 s	2×10^{18}	7.7×10^{-6}	[44]
Pt/Ti	As deposited	5×10^{18}	1.1×10^{-4}	[45]
Pt/Ti	450 °C – 30 s	5×10^{18}	8.0×10^{-7}	[45]
Au/Pt/Ti	450 °C – 30 s	1×10^{18}	8×10^{-6}	[46]
WSi	RT to 600 °C – 2 min	1.4×10^{20}	1.0×10^{-6}	[47]
Ag	400 °C – 3 min	1.7×10^{18}	2×10^{-6}	[48]

One of the most conventional contacts to n-InP is based on the eutectic compound AuGe, classically used on GaAs surfaces. While very low specific contact resistivities are obtained with it ($\rho_c < 5.10^{-7}$ $\Omega.cm^2$), its low fusion temperature (361 °C) leads to important thermal instabilities of the contacts and poor interfacial morphology [49]. The introduction of a top Ni layer acting as a wetting agent suppressed the agglomeration of the AuGe [50]. The latter presents a double advantage as it also reacts with the InP substrate to form binary compounds that seem to be electrically favorable [51-53]. Although the addition of this layer improved the morphology over AuGe, this stack still suffers from a propensity to spike and to be thermally unstable. This is attributed to the diffusion of Au and can be limited by the addition of a Ni layer at the interface between the AuGe and the semiconductor leading to a final Ni/AuGe/Ni stack [54].

Similarly, other conventional contacts to GaAs have been adapted to InP surfaces. These include solid phase regrowth techniques-based contacts. Among them, the Ge/Pd and Ge/Pt-based contacts are particularly interesting because of their high thermal stabilities [42, 44]. For example, the Ge/Pt/Ge/Pt stack still presents a contact resistivity of 9.15 x 10^{-6} Ω.cm² after a 20h-long aging at 400 °C [44]. Aside from these stacks, we can also cite the gold-free contacts such as Pt/Ti for which the contact resistivity decreases substantially to 8.0 x 10^{-7} Ω.cm² after a rapid thermal processing (RTP) at 450 °C [45]. One of the most remarkable stacks was developed by UCSB and Intel. Combining Al, W, Pd, Ge and Pd the contact resistivity was lowered down to 7.2 x 10^{-8} Ω.cm² after a 60 s-thermal treatment at 450 °C [43].

Classical contacts to p-InGaAs

Table 1.3: Classical contacts stacks, annealing treatment conditions, III-V doping level and resulting specific contact resistivity on p-InGaAs surfaces. When encountered, N/A stands for Not Available

Metallization	Annealing treatment	InGaAs doping level [cm^{-3}]	ρc [$\Omega.cm^2$]	Reference
AuGe	N/A	2.2×10^{18}	8.0×10^{-8}	[55]
Pd/AuGe	N/A	4×10^{19}	4.0×10^{-6}	[55]
Pd/Ge	400 °C – 30 min	1.8×10^{19}	2.3×10^{-6}	[40]
Pt/Ti	As deposited	1.5×10^{19}	3.0×10^{-4}	[56]
Pt/Ti	450 °C – 30 s	1.5×10^{18}	3.4×10^{-8}	[56]
Au/Pd/Ti	450 °C – 20s	1×10^{19}	9.1×10^{-6}	[57]
Au/Pt/Ti	450 °C – 30s	5×10^{18}	5.5×10^{-7}	[46]
Al/W/Ti	450 °C – 30s	2×10^{19}	3.3×10^{-6}	[43]
W	400 °C – 30s	2.5×10^{19}	3.8×10^{-6}	[58]
WZn	500 °C – 10 s	$> 1 \times 10^{18}$	5.0×10^{-6}	[59]
Au/Pt/Ti/Pt	400 °C – 25 s	2×10^{19}	1.1×10^{-7}	[60]
Au/Pd/Ti/Pd	400 °C – 20s	1×10^{19}	1.7×10^{-6}	[57]
Al/Ti/Ge/Pd	405 °C – 60s	2×10^{19}	3.1×10^{-6}	[61]
Al/W/Pd/Ge/Pd	450 °C – 30s	2×10^{19}	2.1×10^{-6}	[43]
Au/Ir/Pd	400 °C – 25 s	2×10^{19}	2.1×10^{-6}	[60]
Au/Pt/Si/Gd	300 °C – 1 min	2×10^{19}	5.6×10^{-6}	[60]
Pt/Si/Gd	300 °C – 1 min	2×10^{19}	4.4×10^{-6}	[60]

As in the case of contacts to n-InP, a wide range of metallizations were investigated on p-InGaAs surfaces. The classical AuGe-based contact presents the same positive electrical characteristics on p-InGaAs as it does on n-InP but also tends to present a poor morphology, to spike and to be thermally unstable. Similarly, Pt/Ti contacts give access to resistivity as low as 3.4×10^{-8} $\Omega.cm^2$ on p-InGaAs surfaces after 30 seconds-RTP at 450 °C but are degraded at temperatures higher than 500 °C [56]. The resistivity decrease is attributed to the diffusion of Ti leading to the formation of binary and ternary Ti-In-As-based compounds. Adding Au or W layers does not help decrease the specific

contact resistivity as it seems completely driven by the Ti/p-InGaAs interface. Aside from these Ti-based metallizations, other gold-free contacts were reported. The latter include Pd, Ge and Pt inter-layers and provide resistivities in the range of 10^{-6} Ω.cm². Among those, the Al/W/Pd/Ge/Pd stack developed by UCSB and Intel is again particularly outstanding as it opens the possibility of integrating a unique metallization with low contact resistance both on n-InP and p-InGaAs [43].

Integration of classical contacts on III-V surfaces

Whatever the chosen metallization, the classical contacts usually rely on similar integration schemes. The latter consist in depositing a resist on the III-V surfaces and in patterning it to open contact regions. After a III-V surface preparation, the above-listed stacks are deposited for example by physical vapor deposition (PVD) or by e-beam evaporation. The lift-off of the resin is then carried out, leaving defined metallic pads on InP or InGaAs as schematically represented in Figure 1.12.

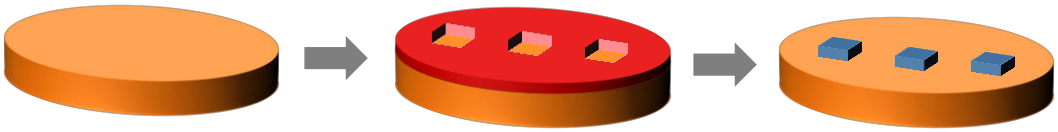


Figure 1.12: Schematic representation of a lift-off integration of contacts.

1.6.2 Transition towards CMOS-compatible contacts

General considerations

Photonics systems could benefit from coupling with silicon substrates but several impediments to a heterogeneous integration exist, especially concerning the contacts. Most of the stacks listed in Table 1.2 and Table 1.3 are comprised of gold which is banned from Si-based CMOS-compatible environments as it acts as a deep-level trap in silicon, therefore hindering the conduction [62]. Because of the additional thermal instability of gold-based metallizations, great efforts were made to develop gold-free contacts. The latter are usually comprised of noble metals which are either prohibited from frond-end microelectronics environments or too expensive to be brought into the world of mass production. Most of them present stacks combining a multitude of layers (up to five) which further complicates their integration. Moreover, most of the above listed contacts require high temperature thermal treatments (T ≥ 450 °C) which would be harmful to the quantum wells of the laser's active region. Finally, the integration scheme of the classical contacts requires the use of non-planar processes such as the lift-off because of the difficulty to etch and to chemically-physically polish most noble metals. As a consequence, both the composition and the integration scheme of the classical contacts appear to be unsuitable to a front-end microelectronics environment.

The combination of these various assessments clearly highlights the fact that the classical contacts are not adapted to a front-end silicon microelectronics environment. Thus, the enabling of III/V-Si heterogeneous integration requires the development of innovative contacts, both in terms of integration and composition. A few studies were initiated in the CEA-LETI to develop such contacts in the late 2000's [63-65]. The corresponding contacts were free from any gold, based on Al(Cu), Ni and Ti metals and presented specific contact resistivities ranging from 2×10^{-5} to 1×10^{-4} Ω.cm^2. However, numerous developments concerning the integration and the optimization of such contacts were still necessary to enable the co-integration of III-V lasers and Si-photonics circuits.

The IRT Photonique project

The *IRT Photonique* project, in the frame of which this PhD was conducted, aims to develop fully integrate III-V / Si heterogeneous photonic devices. More precisely, the purpose of this project is to enable the integration of III-V lasers on the patterned Si-photonics wafers, firstly in 200 mm and ultimately in 300 mm. As already mentioned, permitting the co-integration of III-V active devices with silicon passive ones requires the fulfillment of both a photonics platform's requirements and those of a front-end silicon environment. Among others, because of the incompatibility of classical contacts with a Si-microelectronics environment, innovative contacts must be developed. On top of the requirements already detailed in section 1.6.1, these innovative contacts must meet the following requisites to be integrated on Si-photonics devices:

- Contacts must be integrated thanks to Si-microelectronics compatible and planar processes which exclude any lift-off or related processes;
- Contacts must be integrated thanks to 200 or 300 millimeters-compatible equipment's;
- Stacks must be comprised of front-end compatible materials only, such as Ni, Ti and their alloys;
- All thermal budget must be minimized ($T \leq 450$ °C) in order not to degrade the active region of the laser composed of multi quantum wells (MQW);
- The metallization must be selected to form ohmic contacts (see Chapter 4 for a detailed definition) and must present the lowest sheet resistance, therefore limiting their contribution to the overall resistance. Limit values of series resistance in the overall laser device are about 5 Ω, which induces a maximum of 0.5 to 1 Ω for each contact to minimize the Joule effect and the power consumption. Given the dimensions of the contacts detailed in Figure 1.8, the corresponding specific contact resistivities must be lower than 5.10^{-5} Ω.cm². A higher contact resistivity would cause a local heating of the laser that may give rise to a wavelength shift of the produced photons [66-69].

Taking into account the intrinsic limitations linked to the electrical performances of the contacts as well as those linked to the functioning of the laser, this PhD thesis will be dedicated to the development of front-end Si-microelectronics compatible contacts to p-InGaAs and n-InP. Chapter 2 will present the development of the corresponding integration scheme while a particular focus will be paid to the metal in intimate contact with the III-V semiconductor, *i.e.,* the metallization in the following chapters. The metallization will indeed be metallurgically studied in Chapter 3 while the electrical properties of the integrated contacts will be presented in Chapter 4.

1.7 Conclusion

In this chapter, we presented the benefits of using optic links and photonics, and how they can answer the new communication needs in terms of delay, power, bandwidth and delay uncertainty. We also highlighted the fact that co-integrating III-V compounds with Si is the key to benefit from both the active properties of the III-V compounds and from the thorough knowledge of silicon technologies and processes. While the majority of the components are patterned in a SOI wafer, the emitting device is composed of III-V materials. As a consequence, this laser must be integrated on top of the SOI wafer, in front of the optical entrance of the circuit. Although several techniques are available, ST Microelectronics and the CEA-LETI chose to directly bond it because of their high level of expertise concerning this technique. The functioning of the laser being based on the stimulated emission of photons, one must be very careful about the losses that could be generated. The LASER effect exists as long as the gain, *i.e.* the light amplification, is higher than these losses. To maximize the gain, charge carriers and photons are trapped thanks to quantum wells and thicker layers in a separated confinement heterostructure. The optical losses sources, however, are numerous and range from internal absorption loss and scattering loss to metal or radiation loss. Their minimization can only be achieved by carefully choosing the materials, *i.e.* metals and dielectrics, that surround the III-V laser and by optimizing the integration processes. In order to maximize the laser yield, the contacts which are used to electrically pump it are determining. Unfortunately, the contacts that were classically used up to now are not compatible with a Si-compatible environment and thus with the overall integration chosen by STMicroelectronics and the CEA-LETI. As a consequence, it is of crucial importance to develop innovative contacts that meet the requirements of such an environment while optimizing the performances of the laser device.

CHAPTER 1 - Bibliographic references

[1] ITRS. International Technology Roadmap for Semiconductor, Technical Reports - interconnect. In *ITRS*, 2011.

[2] ITRS. International Technology Roadmap for Semiconductor, Technical Reports - interconnect. In *ITRS*, 2013.

[3] P. Kapur and K. C. Saraswat. Comparisons between electrical and optical interconnects for on-chip signaling. In *Proceedings of the IEEE 2002 International Interconnect Technology Conference, 2002.*, pages 89–91, 2002.

[4] T. Barwicz, H. Byun, F. Gan, C. W. Holzwarth, M. A. Popovic, P. T. Rakich, M. R. Watts, E. P. Ippen, F. X. Kärtner, H. I. Smith, J. S. Orcutt, R. J. Ram, V. Stojanovic, O. O. Olubuyide, J. L. Hoyt, S. Spector, M. Geis, M. Grein, T. Lyszczarz, and J. U. Yoon. Silicon photonics for compact, energy-efficient interconnects invited. *J. Opt. Netw.*, 6(1):63–73, Jan 2007.

[5] D. A. B. Miller. Device requirements for optical interconnects to silicon chips. *Proceedings of the IEEE Photonics in Switching*, 97(7):1166–1185, July 2009.

[6] A.V. Krishnamoorthy, K.W. Goossen, W. Jan, Xuezhe Zheng, R. Ho, Guoliang Li, R. Rozier, F. Liu, D. Patil, J. Lexau, H. Schwetman, Dazeng Feng, M. Asghari, T. Pinguet, and J.E. Cunningham. Progress in low-power switched optical interconnects. *IEEE Journal of Selected Topics in Quantum Electronics*, 17(2):357–376, March 2011.

[7] F. Boeuf. Recent progress on silicon photonics R&D and manufacturing on 300mm wafer platform. In *Colloque MINOS*, 2015.

[8] R. A. Soref and J. P. Lorenzo. Single-crystal silicon: a new material for 1.3 and 1.6 µm integrated-optical components. *Electronics Letters*, 21(21):953–954, October 1985.

[9] R. Soref and J. Larenzo. All-silicon active and passive guided-wave components for lambda = 1.3 and 1.6 µm. *IEEE Journal of Quantum Electronics*, 22(6):873–879, Jun 1986.

[10] D. Fehly, A. Schlachetzki, A. S. Bakin, A. Guttzeit, and H. H. Wehmann. Monolithic InGaAsP optoelectronic devices with silicon electronics. *IEEE Journal of Quantum Electronics*, 37(10):1246–1252, Oct 2001.

[11] L. Czornomaz, E. Uccelli, M. Sousa, V. Deshpande, V. Djara, D. Caimi, M. D. Rossell, R. Erni, and J. Fompeyrine. Confined epitaxial lateral overgrowth (CELO): A novel concept for scalable

integration of CMOS-compatible InGaAs-on-insulator MOSFETs on large-area Si substrates. In *2015 Symposium on VLSI Technology (VLSI Technology)*, pages T172–T173, June 2015.

[12] Z. Wang, C. Junesand, W. Metaferia, C. Hu, L. Wosinski, and S. Lourdudoss. III-Vs on Si for photonic applications: A monolithic approach. *Materials Science and Engineering: B*, 177(17):1551 – 1557, 2012.

[13] G. Roelkens, L. Liu, J. Brouckaert, J. Van Campenhout, F. Van Laere, D. Van Thourhout, and R. Baets. Wafer bonding and heterogeneous integration: III-V/silicon photonics. *14th European Conference on Integrated Optics*, 2008.

[14] D. Liang, J. E. Bowers, D. C. Oakley, A. Napoleone, D. C. Chapman, C.-L. Chen, P. W. Juodawlkis, and O. Raday. High-quality 150 mm InP-to-Silicon epitaxial transfer for silicon photonic integrated circuits. *Electrochemical and Solid-State Letters*, 12(4):H101–H104, 2009.

[15] Alexander W. Fang, Hyundai Park, Ying hao Kuo, Richard Jones, Oded Cohen, Di Liang, Omri Raday, Matthew N. Sysak, Mario J. Paniccia, and John E. Bowers. Hybrid silicon evanescent devices. *Materials Today*, 10:28 – 35, 2007.

[16] T. Okumura, T. Maruyama, H. Yonezawa, N. Nishiyama, and S. Arai. Injection-type GaInAsP-InP-Si distributed-feedback laser directly bonded on Silicon-On-Insulator substrate. *IEEE Photonics Technology Letters*, 21(5):283 – 285, 2009.

[17] Albert Einstein. Zur quantentheorie der strahlung" (On the quantum theory of radiation). *Physika Zeitschrift*, 18:121–128, 1917.

[18] M. Razeghi. High-power laser diodes based on InGaAsP alloys. *Nature*, 369(6482):631–633, June 1994.

[19] G. Roelkens, D. Van Thourhout, R. Baets, R. Nötzel, and M. Smit. Laser emission and photodetection in an InP/InGaAsP layer integrated on and coupled to a silicon-on-insulator waveguide circuit. *Opt. Express*, 14(18):8154–8159, Sep 2006.

[20] Chen Ting, Hong Tao, Pan Jiao-Qing, Chen Wei-Xi, Cheng Yuan-Bing, Wang Yang, Ma Xiao-Bo, Liu Wei-Li, Zhao Ling-Juan, Ran Guang-Zhao, Wang Wei, and Qin Guo-Gang. Electrically pumped room-temperature pulsed InGaAsP-Si hybrid lasers based on metal bonding. *Chinese Physics Letters*, 26(6):064211, 2009.

[21] Xiankai Sun, Avi Zadok, Michael J. Shearn, Kenneth A. Diest, Alireza Ghaffari, Harry A. Atwater, Axel Scherer, and Amnon Yariv. Electrically pumped hybrid evanescent Si/InGaAsP lasers. *Opt. Lett.*, 34(9):1345–1347, May 2009.

[22] A. Bhardwaj, M. Larson, M. Moewe, and Y. Feng. Low-loss InGaAsP/InP surface ridge waveguides for photonic integrated circuits. *IEEE Photonics Technology Letters*, 28(13):1403–1405, July 2016.

[23] A. Kasukawa, R. Bhat, C. E. Zah, M. A. Koza, and T. P. Lee. Very low threshold current density 1.5 μm GaInAs/AlGaInAs graded index separated confinement heterostructure strained quantum well laser diodes grown by organometallic chemical vapor deposition. *Applied Physics Letters*, 59(20):2486–2488, 1991.

[24] Alexander W. Fang, Richard Jones, Hyundai Park, Oded Cohen, Omri Raday, Mario J. Paniccia, and John E. Bowers. Integrated AlGaInAs-silicon evanescent racetrack laser and photodetector. *Opt. Express*, 15(5):2315–2322, Mar 2007.

[25] Berger, V. Principes physiques des lasers à semiconducteurs. 7:01, 2002.

[26] Maurice G. A. Bernard and Georges Duraffourg. Laser conditions in semiconductors. *physica status solidi (b)*, 1(7):699–703, 1961.

[27] V. Zayets. Si wire waveguides (wavelength=1550 nm). *Spintronics Research Center website*.

[28] Daoxin Dai, Yongbo Tang, and John E Bowers. Mode conversion in tapered submicron silicon ridge optical waveguides. *Opt. Express*, 20(12):13425–13439, Jun 2012.

[29] M. Rosenzweig, M. Mohrle, H. Duser, and H. Venghaus. Threshold-current analysis of InGaAs-InGaAsP multiquantum well separate-confinement lasers. *IEEE Journal of Quantum Electronics*, 27(6):1804–1811, Jun 1991.

[30] L.A. Coldren and S.W. Corzine. *Diode lasers and photonic integrated circuits*. Wiley series in microwave and optical engineering. Wiley, 1995.

[31] J. Piprek. *Semiconductor Optoelectronic Devices, Introduction to Physics and Simulation*. 2003.

[32] C. Henry, R. Logan, F. Merritt, and J. Luongo. The effect of intervalence band absorption on the thermal behavior of InGaAsP lasers. *IEEE Journal of Quantum Electronics*, 19(6):947–952, Jun 1983.

[33] C. Bornholdt, W. Döldissen, D. Franke, N. Grote, J. Krauser, U. Niggebrügge, H. P. Nolting, M. Schlak, and I. Tiedke. Passive optical GaInAsP/InP waveguides. *Electronics Letters*, 19(3):81–82, February 1983.

[34] F. Fiedler and A. Schlachetzki. Special issue-optoelectronics optical parameters of InP-based waveguides. *Solid-State Electronics*, 30(1):73 – 83, 1987.

[35] Joris Van Campenhout. *Thin-Film Microlasers for the Integration of Electronic and Photonic Integrated Circuits*. PhD thesis, 2007.

[36] P. B. Johnson and R. W. Christy. Optical constants of transition metals: Ti, V, Cr, Mn, Fe, Co, Ni, and Pd. *Phys. Rev. B*, 9:5056–5070, Jun 1974.

[37] M. A. Ordal, L. L. Long, R. J. Bell, S. E. Bell, R. R. Bell, R. W. Alexander, and C. A. Ward. Optical properties of the metals Al, Co, Cu, Au, Fe, Pb, Ni, Pd, Pt, Ag, Ti, and W in the infrared and far infrared. *Appl. Opt.*, 22(7):1099–1119, Apr 1983.

[38] Edward D. Palik. *Handbook of Optical Constants of Solids*. Academic Press, 1991.

[39] J. Dunn and G. B. Stringfellow. Annealed AuGe based ohmic contacts on InP with ion milling prior to metallization. *Journal of Electronic Materials*, 19(2):L1–L3, February 1990.

[40] W.X Chen, S.C Hsueh, P.K.L Yu, and S.S Lau. Solid-phase epitaxial Pd/Ge ohmic contact to $In_{1-x}Ga_xAs_yP_{1-y}$/InP. *IEEE Electron Device Letter*, EDL-7(8), August 1986.

[41] G. Stremsdoerfer, C. Calais, J.R. Martin, and P. Clechet. Low resistance ohmic contacts onto n-InP by palladium electroless bath deposition. *Journal of The Electrochemical Society*, 137(3):835, 1990.

[42] P. Jian, D. G. Ivey, R. Bruce, and G. Knight. Ohmic contact formation in palladium-based metallizations to n-type InP. *Journal of Electronic Materials*, 23(9):953–962, September 1994.

[43] S. Jain, M. Sysak, M. Swaidan, and J. Bowers. Silicon fab-compatible contacts to n-InP and p-InGaAs for photonic applications. *Applied Physics Letters*, 100(20):201103, 2012.

[44] W-C Huang, T-F Lei, and C-L Lee. PtGe ohmic contact to n-type InP. *Journal of Applied Physics*, 78(10):6108, 1995.

[45] A. Katz, B. E. Weir, S. N. G. Chu, P. M. Thomas, M. Soler, T. Boone, and W. C. Dautremont-Smith. Pt/Ti/n-InP nonalloyed ohmic contacts formed by rapid thermal processing. *Journal of Applied Physics*, 67(8):3872, 1990.

[46] A. Katz, B. E. Weir, and W. C. Dautremont-Smith. Au/Pt/Ti contacts to p-$In_{0.53}Ga_{0.47}As$ and n-InP layers formed by a single metallization common step and rapid thermal processing. *Journal of Applied Physics*, 68(3):1123, 1990.

[47] F. Ren, M. J. Antonell, C. R. Abernathy, S. J. Pearton, J. R. LaRoche, M. W. Cole, J. R. Lothian, and R. W. Gedridge. Nonalloyed high temperature ohmic contacts on Te-doped InP. *Applied Physics Letters*, 74(13):1845, 1999.

[48] V.G. Weizer, N.S. Fatemi, and A.L Korenyi-Both. Sinterless contacts to shallow junction InP solar cells. *Fourth International Conference on Indium Phosphide and Related Materials, 1992.*, pages 318–321, April 1992.

[49] T. Sands. Compound semiconductor contact metallurgy. *Materials Science and Engineering: B*, 1(3):289 – 312, 1989.

[50] Y. C. Shih, M. Murakami, E. L. Wilkie, and A. C. Callegari. Effects of interfacial microstructure on uniformity and thermal stability of AuNiGe ohmic contact to n-type GaAs. *Journal of Applied Physics*, 62(2):582–590, 1987.

[51] M. F. O'Keefe, R. E. Miles, and M. J. Howes. Nickel in ohmic contacts to indium phosphide. *Proceedings SPIE*, 1144:361–367, 1989.

[52] RJ Graham and JW Steeds. Microstructural investigation of large area and device size AuGeNi contacts on InP. *INSTITUTE OF PHYSICS CONFERENCE SERIES*, 67:507–512, 1983.

[53] J. Morais, T. A. Fazan, R. Landers, and E. A. S. Sato. Ohmic contacts formation on n-inp. *Journal of Applied Physics*, 79(9):7058–7061, 1996.

[54] T. C. Shen, G. B. Gao, and H. Morkoc. Recent developments in ohmic contacts for III-V compound semiconductors. *Journal of Vacuum Science & Technology B*, 10(5):2113–2132, 1992.

[55] M. Cooke. Making III-V contact with silicon substrates. *Semicon. Today Compounds and Advanced Si*, 6, May 2011.

[56] A. Katz, W. C. Dautremont-Smith, S. N. G. Chu, P. M. Thomas, L. A. Koszi, J. W. Lee, V. G. Riggs, R. L. Brown, S. G. Napholtz, J. L. Zilko, and A. Lahav. Pt/Ti/p-$In_{0.53}Ga_{0.47}As$ low-resistance

nonalloyed ohmic contact formed by rapid thermal processing. *Applied Physics Letters*, 54(23):2306, 1989.

[57] E. F. Chor, W. K. Chong, and C. H. Heng. Alternative (Pd,Ti,Au) contacts to (Pt,Ti,Au) contacts for $In_{0.53}Ga_{0.47}As$. *Journal of Applied Physics*, 84(5):2977, 1998.

[58] D.Y Kim, J.S Yu, S.J Bae, J.D Song, J.M Kim, and Y.T Lee. Thermally stable tungsten ohmic contact to p-InGaAs and effective barrier height measurement by using the I-V-T method. *Journal-korean physical society*, 38:236–241, 2001.

[59] A. Katz, A. El-Roy, A. Feingold, M. Geva, N. Moriya, S. J. Pearton, E. Lane, T. Keel, and C. R. Abernathy. W(Zn) selectively deposited and locally diffused ohmic contacts to p-InGaAs/InP formed by rapid thermal low pressure metalorganic chemical vapor deposition. *Applied Physics Letters*, 62(21):2652, 1993.

[60] A. Bengi, S.J. Jang, C.I. Yeo, T. Mammadov, S.Ozcelik, and Y.T. Lee. Au and non-Au based rare earth metal-silicide ohmic contacts to p-InGaAs. *Solid-State Electronics*, 61(1):29 – 32, 2011.

[61] W. L. Chen. Ohmic contact study for quantum effect transistors and heterojunction bipolar transistors with InGaAs contact layers. *Journal of Vacuum Science & Technology B: Microelectronics and Nanometer Structures*, 10(6):2354, November 1992.

[62] M.D. McCluskey and E.E. Haller. *Dopants and Defects in Semiconductors*. Taylor & Francis, 2012.

[63] J.-M. Fedeli H. MD Sohrab F. Mandorlo, P. Rojo Romeo and R. Orobtchouk. Mode density reduction and coupling in microdisk lasers processed on a 200-mm cmos pilot line. (17), 2011.

[64] D. Marris-Morini L. Vivien R. Orobtchouk P. Rojo-Romeo C. Seassal J. M. Fedeli, L. Di Cioccio and F.Mandorlo. Development of silicon photonics devices usingmicroelectronic tools for the integration on top of a cmoswafer. 2008.

[65] L. Grenouillet, A.L. Bavencove, T. Dupont, J. Harduin, P. Philippe, P. Regreny, F. Lelarge, K. Gilbert, P. Grosse, and J.M. Fedeli. Cmos compatible contacts and etching for inp-on-silicon active devices. *2009 6th IEEE International Conference on Group IV Photonics*, 2009.

[66] Y.P. Varshni. Temperature dependence of the energy gap in semiconductors. *Physica*, 34(1):149 – 154, 1967.

[67] S. Paul, J. B. Roy, and P. K. Basu. Empirical expressions for the alloy composition and temperature dependence of the band gap and intrinsic carrier density in $Ga_xIn_{1-x}As$. *Journal of Applied Physics*, 69(2):827–829, 1991.

[68] N. K. Dutta and R. J. Nelson. Temperature dependence of threshold of InGaAsP/InP double-heterostructure lasers and auger recombination. *Applied Physics Letters*, 38(6):407–409, 1981.

[69] J. Piprek. Advanced analysis of high-temperature failure mechanisms in telecom lasers. *Proceedings SPIE*, 4533:70–81, 2001.

CHAPTER 2

THE ELECTRICAL PUMPING OF THE III-V LASER: HOW TO INTEGRATE THE CONTACTS IN A SI-COMPATIBLE CLEAN ROOM?

Outline

In the previous chapter we explained the need of external energy supply for the production of photons in the active region of the laser along with issues related to the integration of classical contacts in III/V-Si heterogeneous devices. In this chapter, we will propose alternative solutions for the integration of contacts on each side of the P-N junction, *i.e.* on both n-InP and p-InGaAs surfaces.

2.1 CMOS-compatible contacts integration to III-V surfaces

The classical contacts presented in section 1.6.1, often composed of noble metals and relying on non-planar processes must be replaced in order to develop fully integrated III-V / Si heterogeneous photonic devices. Therefore, innovative contacts meeting the requirements of a functioning laser device and those of a front-end Si-microelectronics clean room must be developed. As a reminder:

- Contacts must be integrated thanks to Si-microelectronics compatible and planar processes which exclude any lift-off or related processes;
- Contacts must be integrated thanks to 200 or 300 millimeters-compatible equipments;
- Stacks must be comprised of front-end compatible materials only, such as Ni, Ti and their alloys;
- All thermal budget must be minimized ($T \leq 450$ °C) in order not to degrade the active region of the laser composed of multi quantum wells (MQW);
- The deposition temperature and the subsequent annealing treatments must be carefully chosen to form interfacial products that lower the contact resistivity while limiting the induced stress;
- The compounds along with their microstructure must be stable up to 450 °C;
- The number of lithography in the integration scheme must be minimized in order to minimize the overall production cost;
- The metallization must be selected to form ohmic contacts with specific contact resistivities lower than 5.10^{-5} Ω.cm².

The development of such contacts requires the implementation of characterization tools. Therefore, in order to determine the electrical and morphological impact of the various processes on the contacts, two different masks were developed as detailed in Table 2.1.

Table 2.1: Recapitulative table of the two masks that were designed in order to characterize and develop the Si-microelectronics compatible contacts to III-V surfaces

	MELT	TASP
Meaning	Mesures Electriques sur structures TLM (Electrical measurements on TLM structures)	TLM structures on As and P-based surfaces
Wafer diameter	50 mm to 100 mm	200 mm
Type of III-V	Bulk III-V substrate (50 mm)	III-V epitaxy (50 mm) bonded on Si wafer (200 mm)

Both masks are composed of 3 different levels of lithography:

- ACTIVE level, used to pattern the III-V stacks and provide electrical isolation of the electrical test structures;
- CONTACT level, used to pattern the contact cavities were the Si-microelectronics compatible metallization is integrated;
- METAL level, used to integrate metallic pads necessary to polarize the contact test structures during the electrical characterization.

While they are quite different from one another, both masks enable the integration of morphological and electrical test structures on III-V surfaces. While the two masks were used to electrically characterize the contacts, the development of the Si-compatible integration scheme and processes presented in this chapter was made solely thanks to the mask TASP. Indeed, only the latter enables the integration of the contacts in a 200 mm-platform, and therefore on 200 mm Si wafers. The corresponding morphological test structures consist in an array of squared contact cavities (5 µm x 5 µm) as shown in the SEM image presented in Figure 2.1.

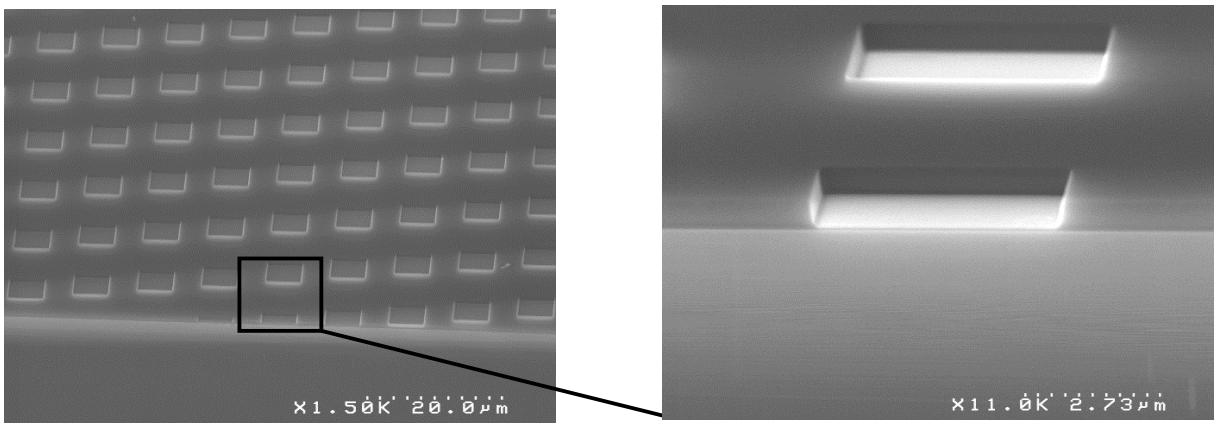


Figure 2.1: Scanning electron microscope (SEM) image of the morphological test structures integrated either on n-InP or p-InGaAs surfaces to develop the CMOS-compatible integration of the contacts.

Because they tend to react very differently, these researches were conducted separately on n-InP and on p-InGaAs surfaces. For the sake of consistency, the stacks that were used for these studies were similar to those present underneath the contacts' regions in the laser (alternating of InP, InGaAsP and InGaAs layers as schematized in Figure 1.8). The resulting epitaxies are displayed in Figure 2.2.

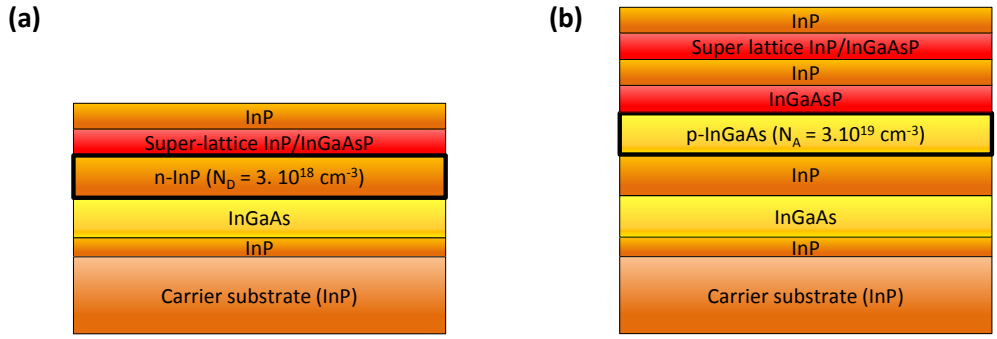


Figure 2.2: Schematic representation of the III-V stacks used for the development of Si-compatible contacts (a) to n-InP and (b) to p-InGaAs surfaces.

These III-V stacks were epitaxially grown on two-inches III-V substrates that were bonded onto 200 millimeters silicon substrates therefore enabling the processing of the wafers in the CEA-LETI's R&D 200 millimeters fab line. The process flow related to the proposed and reviewed integration flow is schematically shown on a laser device in Figure 2.3. In the latter, the contacts are integrated sequentially, starting with those on n-InP. One could also imagine to start with the integration of the contact on p-InGaAs, or to simultaneously integrate the contacts on both surfaces. These different solutions are strongly linked to process conditions such as dry etching, surface cleaning, thermal

budget… In the following sections, we will detail the integration steps, the associated constraints and the proposed solutions which were developed thanks to the morphological test structures [1][1].

[1] Note that some details about the process will not be given in this thesis for the sake of confidentiality.

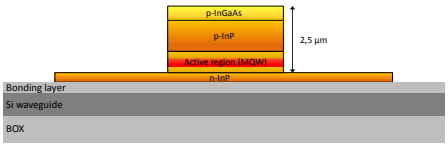
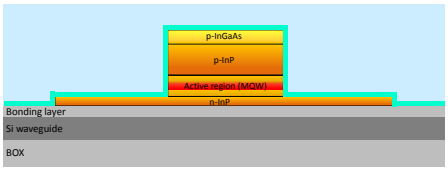
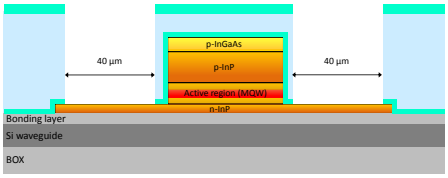
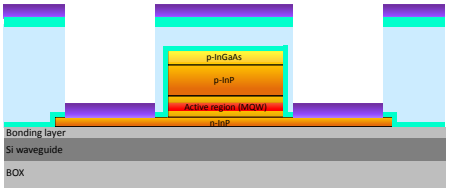
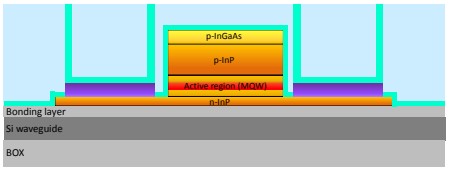
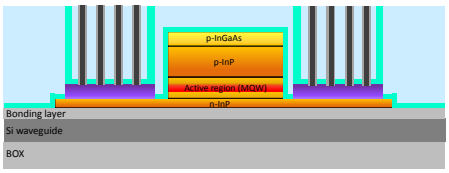
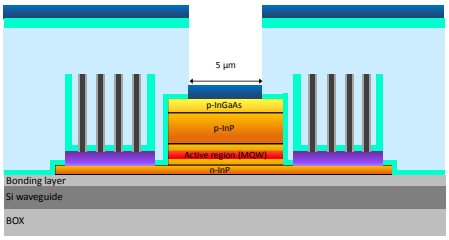
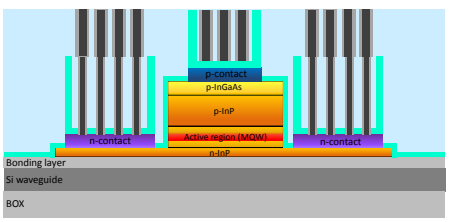
A		Etching of the III-V Laser stack to define the T-shaped active device
B		Dielectric encapsulation CMP planarization
C		First-stage contacts' etching
D		InP surface preparation CMOS compatible metallization deposition
E		SiN and dielectric deposition CMP planarization Thermal annealing (optional)
F		First-stage plugs etching Surface preparation + plugs filling Metal damascene polishing (CMP)
G		Dielectric encapsulation Second-stage contact etching InGaAs surface preparation CMOS compatible metallization deposition
H		SiN and dielectric deposition CMP planarization Thermal annealing (optional) Second-stage plugs etching Surface preparation + plugs filling Metal damascene polishing (CMP)

Figure 2.3: Si-compatible process flow for the integration of the contacts on a III-V laser in the framework of Silicon Photonics. Note that the width of the laser is about 100 µm while its longitudinal dimension is approximately 500 µm.

2.2 Transfer of the III-V stack on the silicon substrate

In STMicroelectronics and in the CEA-LETI, the III-V wafers are transferred on oxidized silicon wafers thanks to the direct bonding process described in section 1.3. To do so, the III-V substrates are carefully chosen as they must present the following characteristics:

- RMS roughness < 0.3 nm on a 1 µm x 1 µm scan;
- Wafer's bow < 10 µm;
- Concentration of defects < 100 cm^{-2};
- Absence of defects longer than 100 nm.

An oxidation of the silicon substrate is made in order to form a 200 nm thick SiO_2 bonding layer. A succession of surface preparations combining wet and plasma treatments are then carried out both on III-V and silicon. The silicon wafer is firstly cleaned in ozonated deionized water to remove the hydrocarbon compounds and make the surface hydrophilic while the III-V wafer is exposed to an ozonated environment. The III-V and SiO_2 surfaces are then exposed to an O_2 plasma which increases the post annealing bonding energy and the III-V wafer is cleaned in deionized water. The two wafers are finally put in contact and a strengthening thermal treatment is carried out at 300 °C for 2 hours under a N_2 atmosphere. The latter converts the Van der Walls bonds into covalent ones between the III-V and the SiO_2. For this study, 2-inches III-V substrate were bonded to 200 mm Si ones as shown in Figure 2.4 (a) along with the corresponding schematic cross sections.

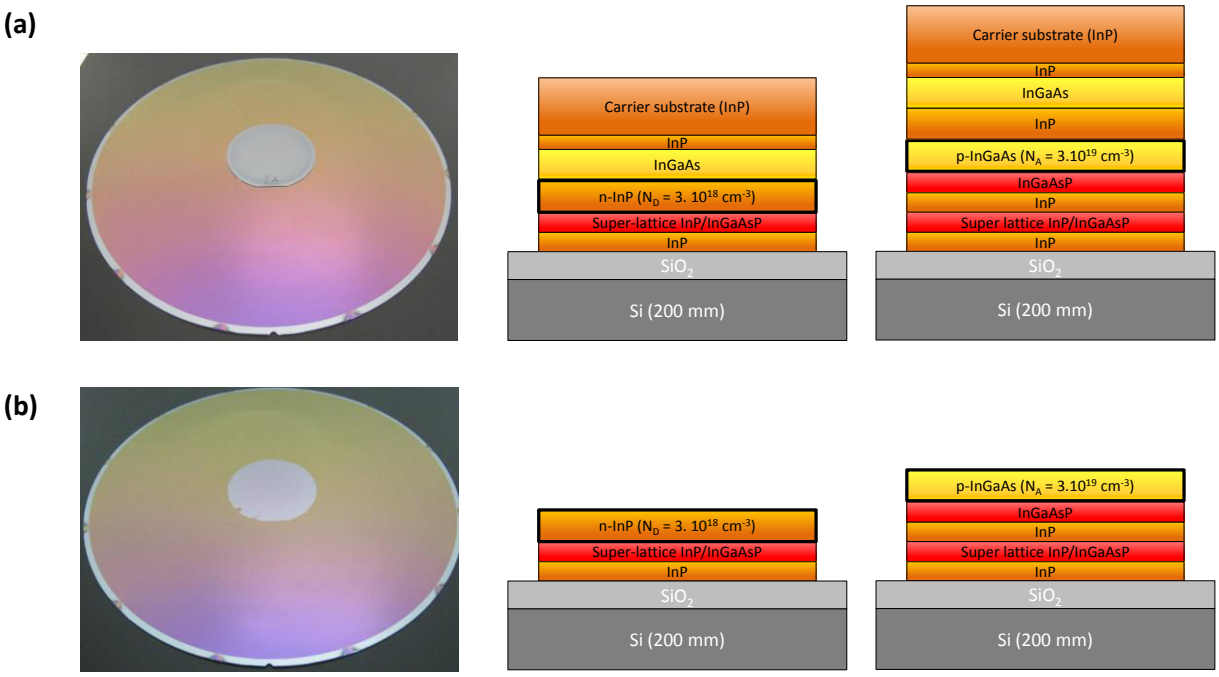


Figure 2.4: Pictures of a 2 inches III-V substrate along with the n-InP and p-InGaAs-based stacks (a) after its bonding to a 200 millimeters oxidized silicon substrate and (b) after the etching of the III-V carrier substrate and of the sacrificial layers.

The III-V carrier substrate is then etched up to the active layers, *i.e.* n-InP or p-InGaAs, thanks to consecutive wet etchings. For this purpose concentrated HCl solutions combined with H_3PO_4 are well adapted to the etching of InP while a mixed solution of H_2SO_4 and H_2O_2 is used to remove InGaAs layers. The final stacks along with the corresponding bonded wafer picture are displayed in Figure 2.4 (b). Note that when reporting full two-inch substrates a great surface of the expensive III-V stack is lost during the subsequent patterning step. In order to minimize the material loss, a solution consists in bonding millimeter-scale dies on the SOI substrate thanks to dedicated holders.

2.3 Etching of the III-V stack via a SiN hard mask

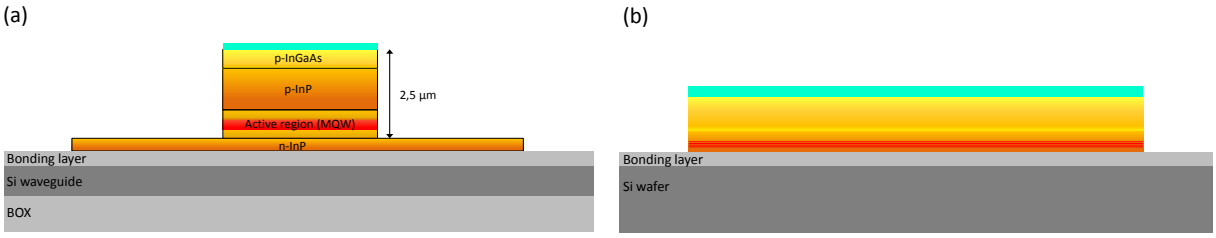


Figure 2.5: Schematic representation of the III-V etching (a) on the III-V laser (b) on the morphological test structures.

After its bonding, the III-V stack is etched to define either electrically isolated squared patterns on the morphological and electrical tests structures or to define the T-shaped laser on the actual devices

(Figure 2.5). The isotropic property of wet chemical etchings makes them unsuitable for this kind of structure patterning. On the contrary directional plasma etchings are well adapted. This kind of process requires the use of a hard mask which acts as a protecting and sacrificial layer during the patterning of the III-V. To fulfill this role, its etching rate must be much smaller than that of the III-V compounds.

Choice of the hard mask

SiN layers are often used as hard masks and must be carefully chosen in order not to deteriorate the surfaces on which the contacts will be integrated afterwards. Additionally, in order not to degrade the active region of the laser, all processes temperatures must not exceed 450 °C. Keeping in mind these restrictions, several types of SiN that are available in the CEA-LETI clean room were selected as listed in Table 2.2.

Table 2.2: Deposition technique and temperature, stress and etching selectivity towards III-V compounds of the available SiN hard masks in the CEA-LETI clean room

	Deposition technique	Deposition temperature	Stress [MPa]
Conformal SiN	PECVD	300 °C	118
Conformal SiN	PECVD	400 °C	-75
Low stress SiN	PECVD	300 °C	-60

While the low stress SiN offers the lowest deposition temperature and intrinsic stress, its availability comes as an issue. For the time being, in the CEA-LETI, its deposition can only be performed in an equipment located in a clean room dedicated to MEMs devices were the contamination level is high compared to that of the CMOS-dedicated clean room, and therefore compared to our application standards[2]. The aim of these studies being to develop a fully CMOS-compatible integration, the use of this low stress SiN was thus not possible during this study. Nevertheless, because of its strong assets we decided not to renounce this option and assessed it optically and electrically in sections 2.4 and 4.6). The two other solutions include conformal SiN deposited either at 300 °C or at 400 °C by plasma enhanced chemical vapor deposition (PEVCD). However, III-V surfaces are known to be sensitive to high temperatures. Thus, to discriminate these two processes and select the most adapted deposition temperature, AFM measurements were performed before and after SiN depositions at 300 °C and 400 °C on InP and InGaAs surfaces (Figure 2.6).

[2] The deposition of the low stress SiN should be available in the CMOS-dedicated clean room at the beginning of 2017.

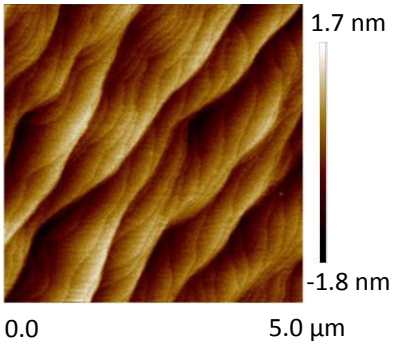
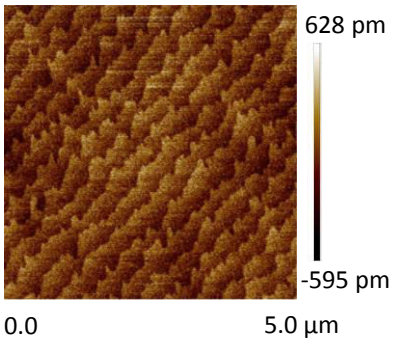
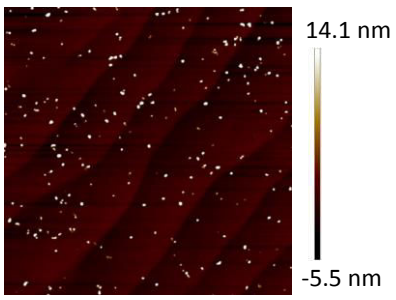
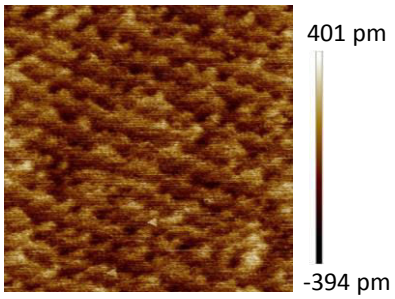
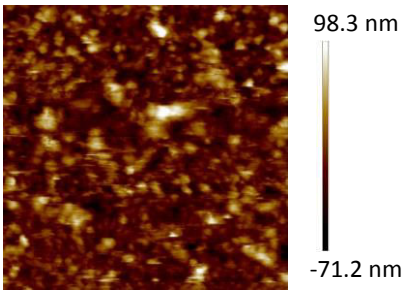
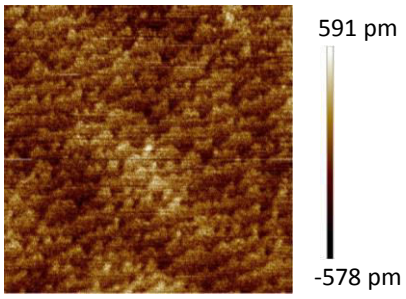
	InP	InGaAs
Reference surfaces		
	RMS roughness = 0.44 nm	RMS roughness = 0.14 nm
After SiN deposition at 300 °C		
	RMS roughness = 0.95 nm	RMS roughness = 0.10 nm
After SiN deposition at 400 °C		
	RMS roughness = 18.9 nm	RMS roughness = 0.13 nm

Figure 2.6: AFM scans (5 µm x 5 µm) of InP and InGaAs surfaces before and after deposition of conformal SiN at 300 °C and 400 °C. The deterioration of InP surfaces at 400 °C is highlighted by the sharp increase of the RMS roughness.

While InGaAs surfaces are not altered by this process, depositing the conformal SiN at 400 °C results in a strong deterioration of InP surfaces. Thus, depositing the hard mask at 400 °C is not adapted to

such surfaces. On the contrary, the 300 °C deposition process does not induce any morphological deterioration of InP and InGaAs surfaces.

Because of the unavailability of the low stress SiN and the deterioration of the surfaces caused by the 400 °C process, the conformal SiN deposited at 300 °C was ultimately retained as the most adapted hard mask for the etching of InP and InGaAs surfaces. In the following, this selected material will be noted *conformal SiN*.

III-V plasma etching

An inductively coupled plasma process (ICP) is used for the patterning of the III-V stack. This kind of plasma etching provides high etching rates (260 to 360 nm/min) which are necessary in the case of the several micrometers thick III-V laser stack (Figure 2.3.A). As highlighted by the scanning electron microscope (SEM) image displayed in Figure 2.7 it also leaves smooth and vertical III-V sidewalls. The minimization of the roughness is essential not to induce scattering losses and therefore not to decrease the emission efficiency of the laser (see section 1.5.2). Consequently, it appears that the use of an ICP process combined with a conformal SiN hard mask deposited at 300 °C are well adapted for the patterning of the III-V stacks in terms of process efficiency and in terms of photon loss minimization.

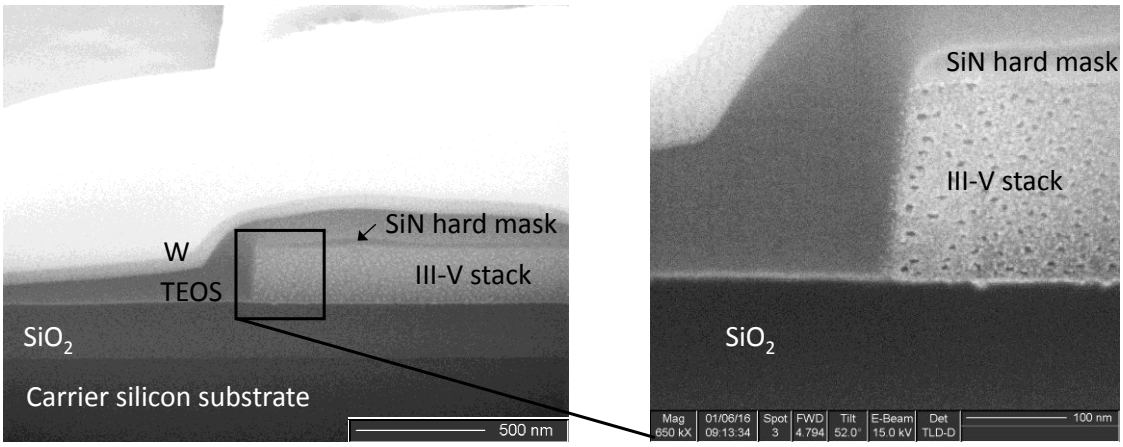


Figure 2.7: SEM (Scanning Electron Microscope) image of a III-V stack (n-InP top layer) after its dry etching via a SiN hard mask prepared using FIB (Focused Ion Beam). The black dots that are present in the InP layer are caused by the SEM characterization and must be disregarded. Note that the TEOS (Tetraethyl orthosilicate) and W were used to protect the structure during the FIB etching.

2.4 Dielectric encapsulation

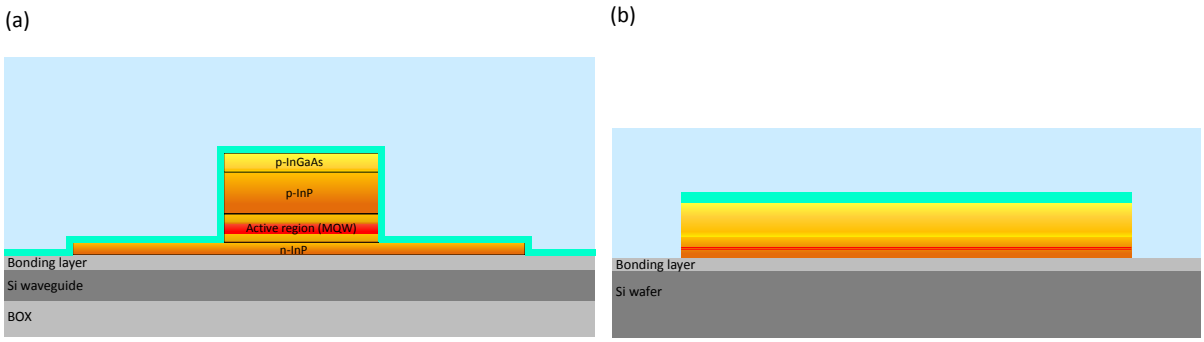


Figure 2.8: Schematic representation of the dielectric encapsulation (a) on the III-V laser and (b) on the morphological test structures.

The planar integration of the contact regions is made possible by an initial dielectric encapsulation of the whole structure. However, the choice of the dielectric nature is crucial because of its vicinity from the laser's active region in the device. In the following sections we will present the optical and thermal characteristics of the dielectric candidates allowing us to determine the best available options for the laser encapsulation.

2.4.1 Criteria for the selection of the candidates

When photons are close to a material which presents a high optical absorbance, they can be extracted from where they are to be absorbed by the second material (see section 1.5.2). In the case of the laser, photons are located in the active region of the III-V laser which is itself contiguous with the dielectric encapsulation as schematized in Figure 2.8. If the latter presents an absorption coefficient higher than the gain coefficient of the laser (typically 3 x 10^3 cm^{-1} to 6 x 10^3 cm^{-1} for InGaAsP/InGaAs or InGaAs/GaAs quantum well structures [2-4]), the losses would become predominant. To minimize them, it is therefore necessary to choose one or several dielectric compounds with a low absorbance at the emitting wavelength of the laser (1.3 – 1.55 µm).

Important losses can additionally be generated by the presence of a high refractive index-material close to the region where photons are located. These are the so called radiation losses described in section 1.5.2. In order to minimize them, the dielectric materials surrounding the III-V active region must present a refractive index lower than that of the III-V stack. The refractive index of InP, InGaAs and InGaAsP being in the range of 3.16 to 3.56, the chosen dielectrics' indexes shall therefore be lower than 3.16 [5-8].

Aside from the optical properties of the dielectric compounds, their propensity to evacuate the heat produced by the operating laser must be considered. When functioning, the device locally warms up which might result in a performance degradation of the laser as well as a wavelength shift of the produced photons [9-12]. The thermal conductivity of the chosen dielectric compounds must therefore be as high as possible. Finally, because a damascene CMP approach is used in this innovative integration scheme, the chosen dielectric compound(s) must be planarizable by CMP.

Based on these criteria, several dielectrics were selected for this study, as summarized in Table 2.3. First of all, the low stress and conformal SiN that were presented as potential hard mask candidates could act as encapsulation materials by increasing their thicknesses. Silicon dioxides (SiO_2) were also selected as their refractive index is known to range from 1.45 to 1.54 (λ = 1.3 – 1.55 µm), and therefore should not be responsible for any radiation loss [13-16]. In the CEA-LETI clean room, SiO_2 layers can be deposited by PEVCD either at 300 °C or at 400 °C. However, we showed in the previous section that the underlying SiN is deposited at 300 °C. Therefore, for the sake of consistency and not to induce any degassing of the SiN, the SiO_2 deposition must be performed at 300 °C. Finally, aluminum oxide (Al_2O_3) which refractive index ranges between 1.57 and 1.7, was primarily selected because of high thermal conductivity values ($K > 40$ $W.m^{-1}.K^{-1}$) reported in the literature for crystalline alumina [16-19]. It is important to note that the ultimate dielectric stack might be composed of a combination of several dielectric compounds in order to benefit from all offered advantages.

Table 2.3: Deposition technique, temperature, rate and thicknesses of the four dielectric compounds that are candidate for the encapsulation of the III-V stacks

Dielectric nature	Deposition technique	Power	Deposition temperature	Deposition rate [nm / min]	Thickness of the layer [nm]
Low stress SiN	PECVD	Single frequency	300 °C	760	2000
Conformal SiN	PECVD	Mixed frequency	300 °C	60	200
SiO_2	PECVD	Single frequency	300 °C	690	2000
Al_2O_3	PVD	--	Room Temperature (RT)	1.9	800

2.4.2 Optical characteristics of the dielectric compounds

Transmittance, Reflectance and Absorbance of the dielectric compounds

The transmittance (T), reflectance (R) and absorbance (A) of the selected dielectrics compounds were measured thanks to a classical setup detailed in Appendix A1. Four wafers were prepared for this experiment with low stress SiN, conformal SiN, SiO_2 and Al_2O_3 deposited layers on 200 mm Si substrates. To minimize the associated error, the corresponding thicknesses were maximized but vary from one dielectric to another because of multiple reasons. The stress of the conformal SiN induces an important strain that could result in a delamination of the layer for a too important thickness. For this reason we decided not to deposit more than 200 nm of this compound. The Al_2O_3 presents a very low deposition rate and not less than 7 hours were necessary to deposit the 800 nm thick layer. The two other dielectrics' depositions don't present any limitation and thicknesses of 2000 nm were deposited. A summary of these details is present in Table 2.3.

Utilizing the setup described in Appendix A1, the reflectance and transmittance coefficients, *i.e.* respectively R and T, were measured for the four dielectrics. Based on these results and on Equation 2.1, the absorbance (A) was calculated.

$$A = 100 - T - R\ [\%] \qquad \textbf{Equation 2.1}$$

The thicknesses of the layers being very different from one another, the direct comparison of the parameter *A* would not be relevant. To account for this difference, the absorption coefficient, noted α, must be calculated for each dielectric/Si couple:

$$\alpha_{diel/Si} = \frac{A}{e/\cos(\theta)}\ [cm^{-1}] \qquad \textbf{Equation 2.2}$$

With A the absorption parameter [%],

e the thickness of the considered layer [cm],

θ the angle of incidence, equal to 7° in our experimental setup [°].

This parameter is plotted as a function of the wavelength for the four probed dielectric compounds in Figure 2.9(a) and (b). As detailed in appendix A1, the Si substrate is absorbent for wavelengths lower than 1.13 µm and transparent for higher wavelengths. Therefore, it does not lead to any photon absorption in the range of the telecommunication wavelengths (1.3 – 1.55 µm). However, the

reflection phenomena are quite complex and might be modified by the presence of a dielectric/Si interface. Therefore, all these experiments were conducted on similar wafers in order not to induce any variability. The absorption coefficient calculated between 1.3 and 1.55 µm for all the dielectric compounds deposited on Si substrates are presented in Figure 2.9 (c). The low stress SiN, SiO_2 and Al_2O_3 present absorption coefficients in the range of 500 to 1500 cm^{-1} while the conformal SiN appears to be much more absorbent (4900 cm^{-1} < $\alpha_{conformal\ SiN}$ < 6700 cm^{-1}) between 1.3 and 1.55 µm. As explained before, these absorption coefficients need to be low enough not to compensate the production of photons in the active region of the laser. Considering the fact that typical maximum gains of InGaAsP-based laser devices range from 3000 cm^{-1} to 6000 cm^{-1}, the use of the conformal SiN is not optimal for the encapsulation of the III-V active device. On the other hand, concerning the absorbance properties of the dielectrics, the low stress SiN, SiO_2 and Al_2O_3 would be suitable for this encapsulation.

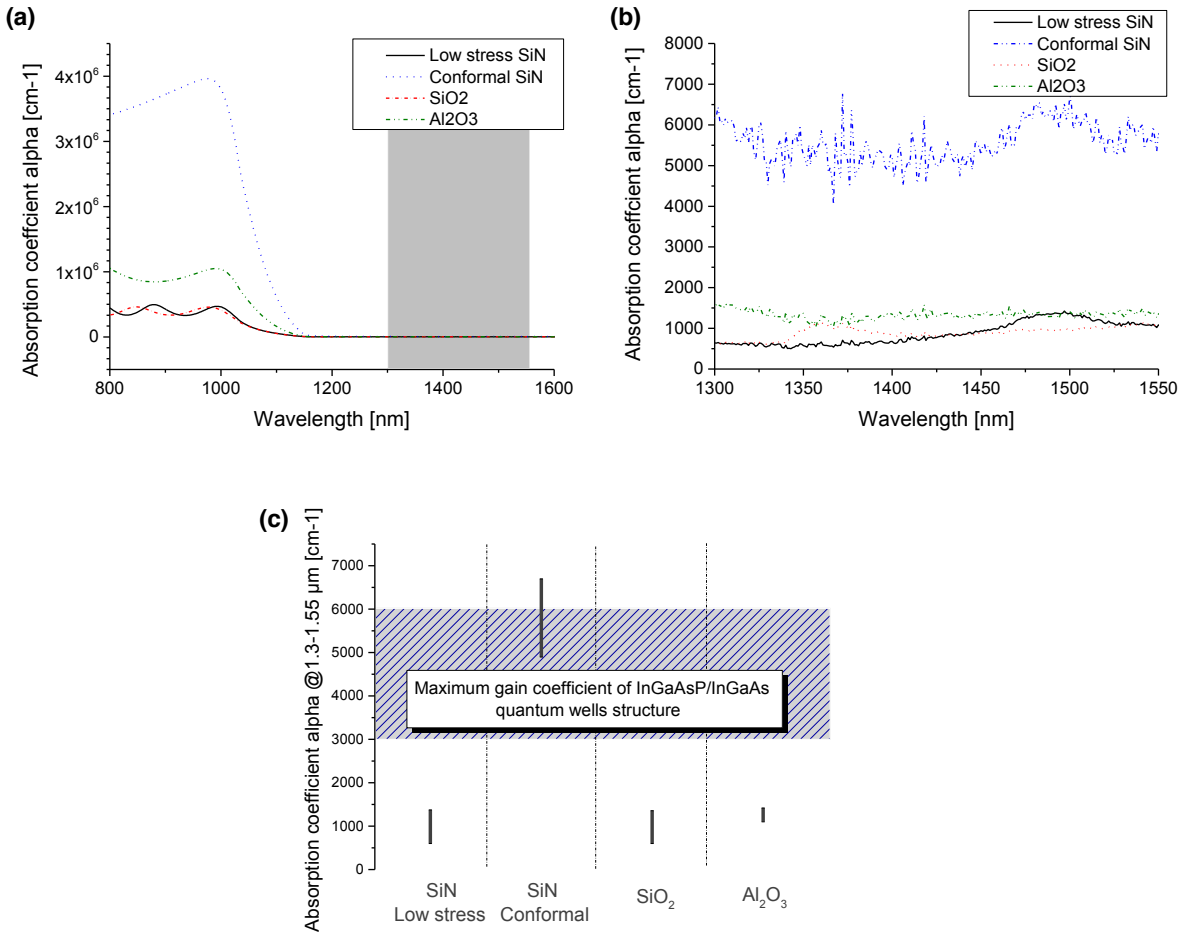


Figure 2.9: Optical absorbance coefficients (α_{diel}) of low stress SiN, conformal SiN, SiO_2 and Al_2O_3 (a) @0.8 – 1.6 µm, (b) zoom on the 1.3-1.55 µm range and (c) comparison of the α_{diel} values with the maximum gain of a InGaAsP/InGaAs quantum wells structure @1.3 - 1.55 µm.

Refractive index of the dielectric compounds

The refractive indexes of the dielectric compounds, noted N, are crucial parameters as they could generate radiation losses if they were superior to those of the III-V active stack. These indexes are a function of the wavelength and of the various characteristics of the considered material such as its crystallography or its dielectric properties. The refractive indexes of the four dielectric compounds were determined thanks to a spectroscopic ellipsometry characterization described in Appendix A2 [20-22]. Such a technique, combined with an additional step of regression, gives access to the optical characteristics of the samples. The experimental results are compared to theoretical models allowing the determination of the complex refractive index of the compound and of layer(s) thickness(es). In the case of absorbent dielectric compounds, the Tauc-Lorentz model is used [23]. As explained in appendix A2, this model presents some limitations which lead us to consider exclusively the real part of the dielectric compounds' refractive index.

In Figure 2.10(b), these refractive indexes are reported and compared to the III-V active stack's ones. The four of them appear to be lower than those of the III-V stack. Therefore, the difference being important enough, none of the dielectric compounds that were probed should generate any radiation loss.

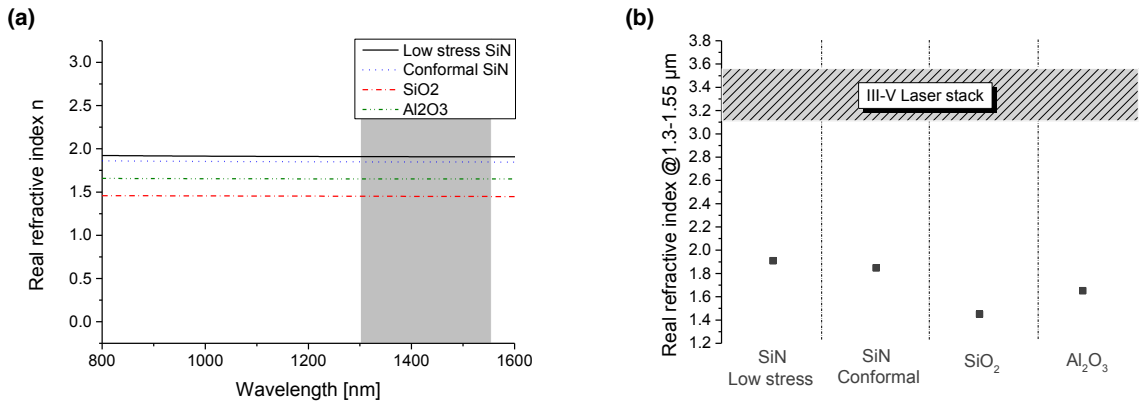


Figure 2.10: Real refractive index of low stress SiN, conformal SiN, SiO_2 and Al_2O_3 (a) plotted as a function of the wavelength between 0.8 and 1.6 µm and (b) between 1.3 and -1.55 µm and comparison with the refractive indexes of the III-V laser stack.

2.4.3 Thermal characteristics of the dielectric compounds

As explained before, while the optical characteristics of the dielectric compounds are of crucial importance, their ability to evacuate the heat produced by the operating laser is also fundamental. To evaluate this point, a bibliographical research was conducted. As the deposition technique strongly influences the thermal conductivities of the materials, a particular attention was given to

this point. The thermal conductivities that are presented in Figure 2.11 therefore correspond to PEVCD – SiN, representing the low stress and conformal SiN, and PECVD - SiO_2 and PVD - Al_2O_3 layers.

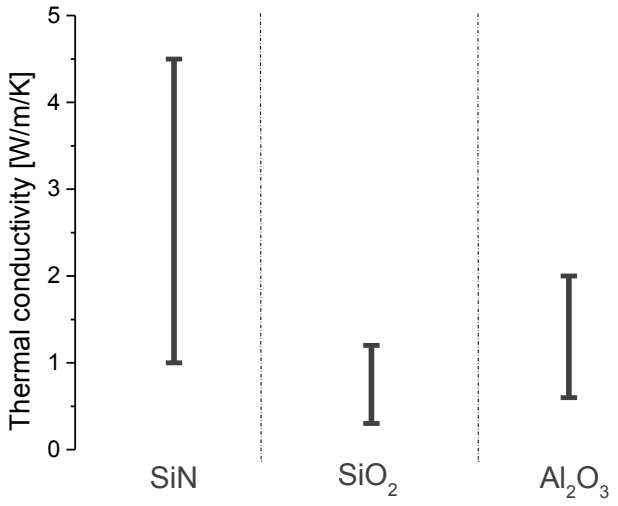


Figure 2.11: Thermal conductivity of PECVD – SiN (corresponding to both conformal and low stress SiN) [24-27], PECVD - SiO_2 [28-37]and PVD - Al_2O_3 [16, 38, 39]

While the Al_2O_3 was primarily selected because high thermal conductivities ($K > 40\ W.m^{-1}.K^{-1}$) were reported in the literature, Figure 2.11 does not display such a characteristic [16-19]. Indeed, these high values were reported for crystalline alumina (α-Al_2O_3) while additional characterizations on our films showed that they are amorphous. Therefore, the thermal conductivities that are reported in Figure 2.11 correspond to amorphous Al_2O_3 deposited by PVD. A recrystallization of the dielectric compound could be made thanks to a thermal treatment after the Al_2O_3 deposition. However, studies report a crystallization temperature above 800 °C to which the laser could not be submitted without being deteriorated [40-42]. Taking into account this restriction, it appears that the available SiN, SiO_2 and Al_2O_3 present comparable and reasonable thermal conductivities. As a consequence, the three compounds would be suitable for the evacuation of the heat produced by the laser.

2.4.4 Summary of the results

The optical and thermal characteristics of low stress SiN, conformal SiN, SiO_2 and Al_2O_3 were reported. It appears that the conformal SiN presents a high absorbance coefficient between 1.3 and 1.55 µm. This feature would lead to an important loss of the produced photons and must thus be avoided for the encapsulation of the III-V laser. Aside from the absorbance coefficients, the refractive indexes of the dielectric compounds were measured. None of the scanned materials would generate radiation losses as all of their refractive indexes are lower than those of the III-V active region. Thus,

concerning the optical properties, the suitable candidates for the encapsulation of the III-V laser would be the low stress SiN, the SiO_2 and the Al_2O_3. The consideration of the thermal characteristics did not restrain the list of candidates as the three of them present similar and suitable thermal conductivities. Because of the present topography on the laser device, a flattening of the dielectric surface must be made thanks to a chemical-mechanical polishing. Unfortunately the planarization of Al_2O_3 can be very challenging and is not controlled yet in many clean rooms, including that of CEA-LETI and STM Crolles. Eventually, because of the additional limitations linked to the restricted availability of low stress SiN, the SiO_2 was selected, for the time being, as the most suitable option for the encapsulation of the laser device.

2.5 Contact cavities opening

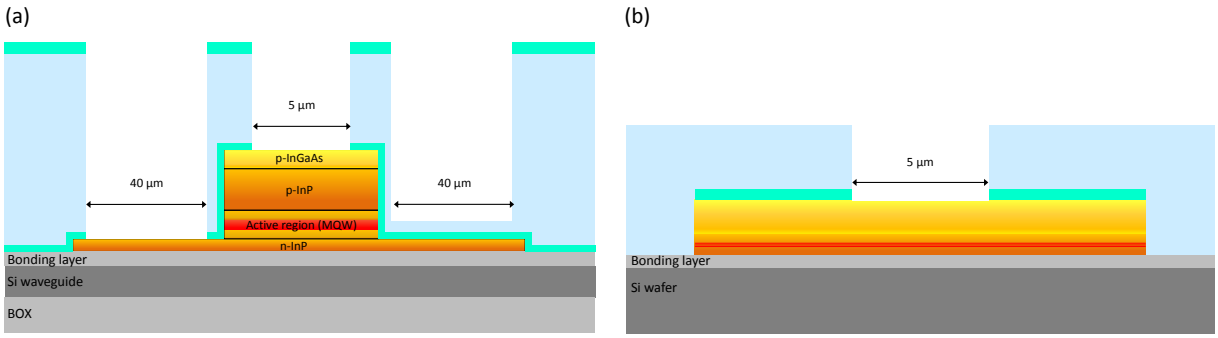


Figure 2.12: Schematic representation of the contact cavities opening (a) on the III-V laser and (b) (b) on the morphological test structures.

Once the III-V stack is encapsulated, the contact cavities have to be opened in the dielectric stack down to the III-V surfaces. This step is one of the most sensitive in this integration flow as it must not deteriorate the n-InP or p-InGaAs surface where the ohmic contacts will be formed afterwards. The corresponding requirements are the following ones:

- The dry etchings must not increase the roughness of the surfaces (RMS roughness < 0.3 nm);
- The surface stoichiometry must not be altered;
- The dry etching process must not leave any residues on the semiconductor surfaces.

Similarly to the etching of the III-V, several micrometers of dielectric have to be removed during this process. Consequently, it requires the use of a hard mask. In order to be coherent in terms of processes and temperatures, and because it appears to be very efficient, the conformal SiN deposited at 300 °C is used. At this point of the integration, the dielectric stack is thus composed of conformal SiN / SiO_2 / conformal SiN / n-InP or p-InGaAs. The top SiN and SiO_2 are firstly etched down

to the bottom SiN etch stop layer. Because of the several micrometers that separate the p-InGaAs and n-InP layers a simultaneous opening of all cavities would require the use of very thick hard masks (t > 1.2 µm). As a consequence, a sequential integration of both contacts might be favored, as represented in Figure 2.3. In any case, while the etchings of SiN/SiO2 are not problematical, the etching of the bottom SiN is very delicate as it could modify the InP and InGaAs surface states. For this purpose, plasma etchings classically used to etch SiN layers on Si or III-V surfaces were selected. Studies were conducted on InP and InGaAs surfaces after the etching processes to determine the most appropriate plasma composition. More precisely, their impact on the surfaces' roughness and stoichiometry were probed thanks to AFM and XPS measurements.

The first tested plasma is a well-known fluoro-carbonated (CH_2F_2) SiN etching usually used on Si surfaces. However, a roughening of the surface along with an increase of the corresponding contact resistance due to residual carbon-containing residues was reported with this plasma [43-45]. As a consequence, a SF_6 plasma, that was proven to etch selectively SiN hard masks on InP surfaces was also tested [46]. While it is often coupled with O_2 to increase the etching rate, we chose to use it on its own not to induce an oxidation of the III/V surface which would degrade the contact resistance [47].

The measurement of InP and InGaAs surfaces' roughness before and after their exposition to the plasma treatments are displayed in Figure 2.13. As indicated by these RMS roughness measurements, the CH_2F_2 plasma does not lead to a deterioration of the surface morphology. The roughness of the InP and InGaAs surfaces are constant or even smaller after the plasma treatment. On the other hand, the SF6 plasma leads to an important increase of the roughness of InGaAs surfaces which is multiplied by three.

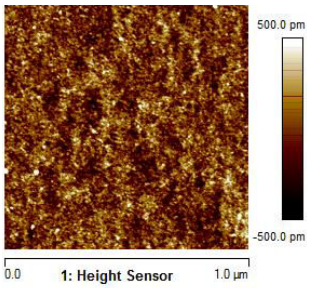
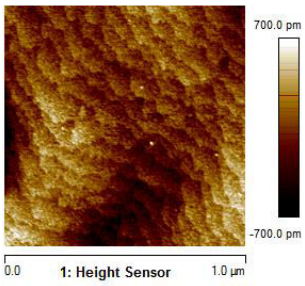
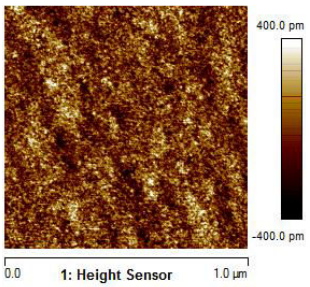
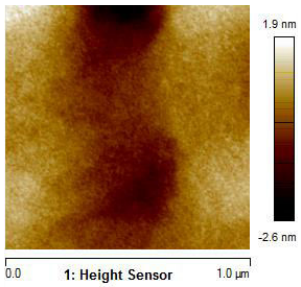
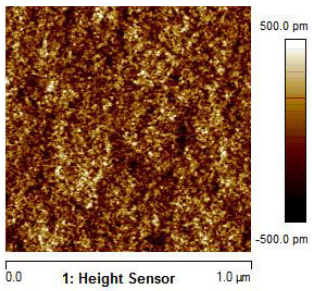
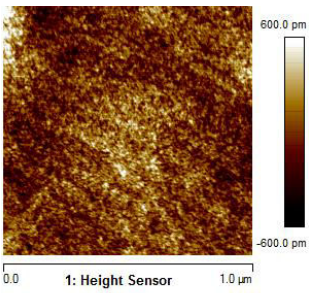
	InP	InGaAs
Reference surfaces		
	RMS roughness = 0.15 nm	RMS roughness = 0.21 nm
SF_6 plasma		
	RMS roughness = 0.13 nm	RMS roughness = 0.64 nm
CH_2F_2 plasma		
	RMS roughness = 0.16 nm	RMS roughness = 0.18 nm

Figure 2.13: AFM measurements (1 µm x 1 µm) of InP and InGaAs surfaces before their exposition to any plasma, after their exposition to a SF_6 plasma and after their exposition to a CH_2F_2 plasma.

The compositions of InGaAs and InP surfaces were also determined thanks to XPS measurements, before and after the plasma treatments. Based on these results, the V/III ratios were calculated and are displayed in Figure 2.14. While both plasma have different effects on the surfaces' morphologies, they tend to modify the stoichiometry in a similar way. The V/III ratios strongly decrease because of important P and As depletion respectively on InP and InGaAs surfaces. This effect is not surprising as the dry etching processes remove atoms thanks to a physical bombardment of the surfaces. This action is very traumatic for III-V surfaces and especially for the light and volatile P and As atoms.

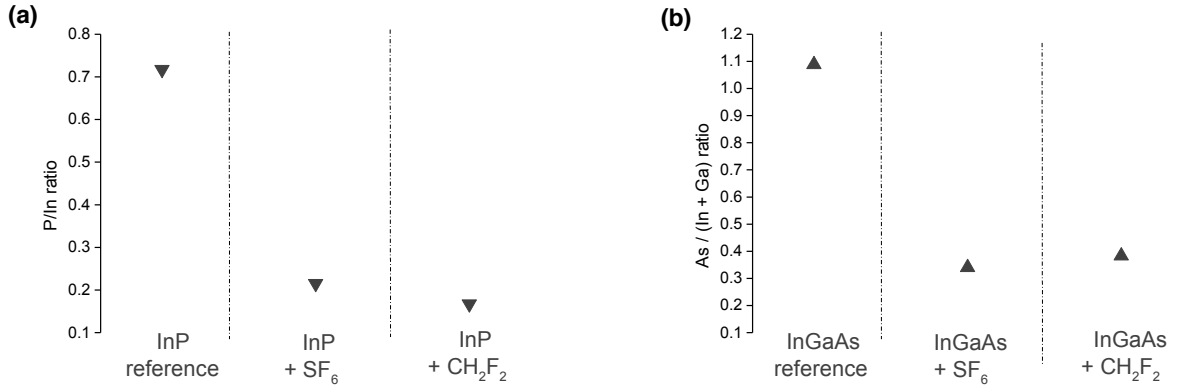


Figure 2.14: V/III ratio of (a) InP and (b) InGaAs surfaces measured by XPS before and after their exposition to CH_2F_2 and SF_6 plasma.

Considering the fact that both available plasma treatments induce a similar change of stoichiometry, but that only the CH_2F_2 does not degrade the surfaces' roughness, the latter was chosen to perform the etching of the bottom SiN. However, additional studies will have to be conducted in order to develop innovative SiN etchings processes that would be less invasive on III-V surfaces. Whatever the plasma composition, the dry etching processes are very traumatic for surfaces as sensitive as InP and InGaAs. One solution might be to use a wet etching keeping in mind that its isotropic property would cause a lateral over-etching of the contact cavities. A compromise would therefore consist in etching most of the bottom SiN thanks to a dry etching process, and then remove the last nanometers thanks to a wet etching, for example composed of diluted hydrofluoric acid (HF).

A cross sectional SEM image of a squared contact cavity (5 µm x 5 µm) defined thanks to the dry etching of the SiN / SiO_2 / SiN dielectric stack is shown in Figure 2.15. In order to ensure the complete removal of the SiN layer, the duration of the etching is calculated (duration = etching rate x thickness) and several seconds are added: this additional time is called the overetching. One can see in Figure 2.15 that in spite of this overetching, no III-V was removed during the process meaning that the CH_2F_2-based process is highly selective towards the III-V compounds.

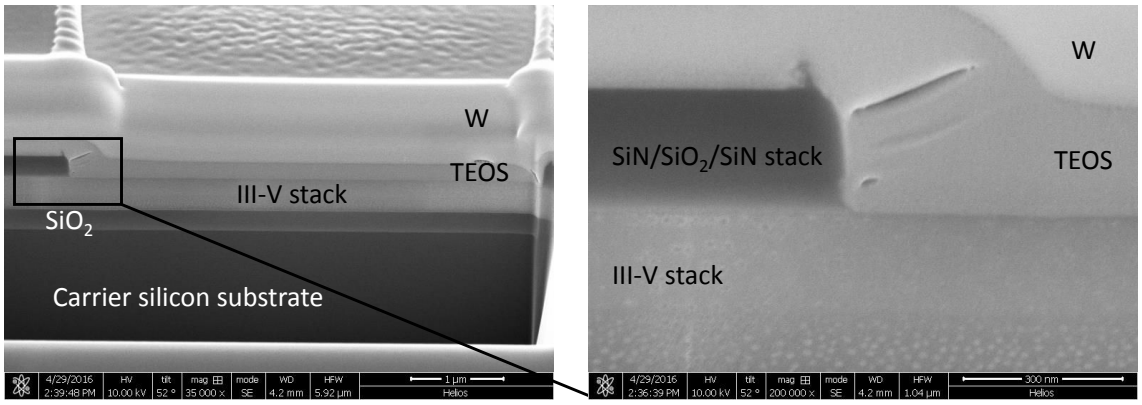


Figure 2.15: FIB/SEM image of a contact cavity (5µm x 5 µm; p-InGaAs top layer) after the dry etching of the SiN/SiO_2/SiN dielectric stack. The white dots that are present in the InP layer are only caused by the SEM characterization. Note that the TEOS and W were used for the FIB etching only.

However, an additional SEM characterization in top view highlighted the presence of SiN residues on the III-V surface Figure 2.16(a). The removal of this kind of residues has been extensively studied and HF solutions are generally very efficient [48-51]. Therefore we chose to use a highly diluted HF solution in order not to induce any etching of the SiN present in the walls which would increase the lateral dimensions of the cavities. As shown in Figure 2.16, all the SiN residues were efficiently removed from the III-V thanks to a 60-seconds HF (0.1 %) wet treatment.

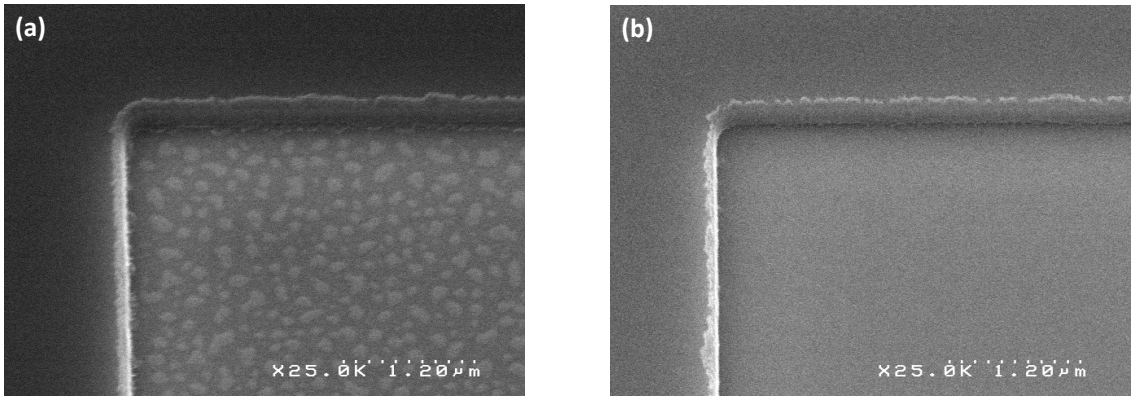


Figure 2.16: SEM image of a contact cavity opened down to an InGaAs surface thanks to a CH_2F_2 dry etching (a) before a wet treatment (b) after a wet treatment in diluted HF (0.1 %) for 60 s.

2.6 III-V surface preparation and CMOS-compatible contact metallization

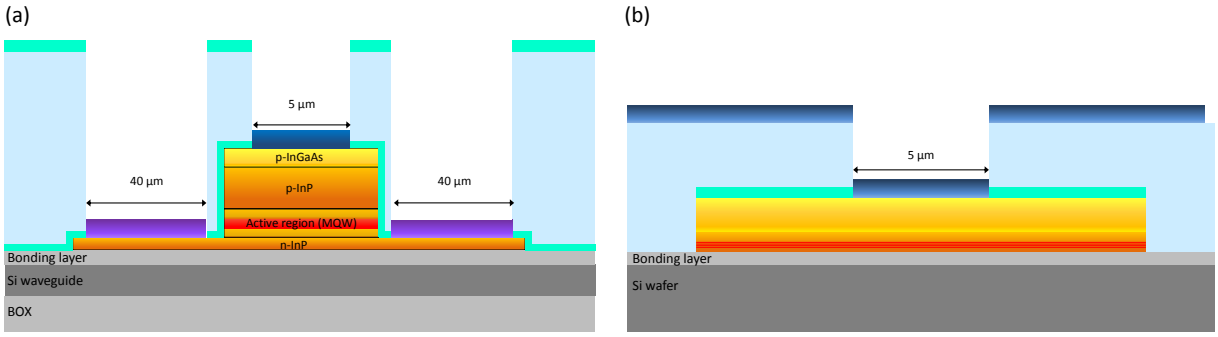


Figure 2.17: Schematic representation of the integrated contact metallization (a) on the III-V laser and (b) (b) on the morphological test structures.

The contact cavities being etched down to the III-V surfaces, *i.e.*, n-InP or p-InGaAs, the CMOS-compatible metallization can be integrated. In order to minimize the resulting contact resistivity, this integration is decomposed in two main steps: a surface preparation is carried out in order to suppress all contaminants and oxides from the InP and InGaAs before the deposition of the CMOS-compatible metals forming the contact. In the frame of this innovative integration scheme, it was chosen to differentiate the integration of the metal in contact with the semiconductor (*i.e.* the metallization) and the filling metal used to bring the current down to the interface (*i.e.* the plug). By doing so, the tuning of the interface metallurgical and electrical properties is facilitated as fewer processes and materials interfere. In the following sections we will firstly detail the surface preparation that we developed along with the various strategies that were identified for the integration of the metals that compose the contact.

2.6.1 III-V surface preparation

The III-V surface being very reactive when exposed to oxygen, a two-step surface preparation is carried out to suppress contaminants and oxides. The first step consists in a wet surface preparation and the second in a plasma treatment. The latter is carried out in the equipment were the metallization is deposited, therefore avoiding any air break and as a consequence preventing any oxide regrowth.

Wet surface preparation

The wet preparation of III-V surfaces is well referenced in the literature. While various chemical compositions were tested and reported, the criteria used to determine whether a wet treatment is suitable or not are the following [52]:

- The wet treatments must be ESH (Environment, Security, Health)-compatible;
- The wet treatments must not increase the roughness of the surfaces (RMS roughness < 0.3 nm);
- The particles and metallic contamination must be removed;
- The oxides must be removed either without etching the III-V compounds or by means of a controlled etching of the surface;
- The surface stoichiometry must not be altered.

In order to meet the previously listed requisites and based on literature, two HCl-based wet treatments were tested both on n-InP and p-InGaAs surfaces [52-55]:

- HCl (37 %) : H_2O = 1 : 2 ([HCl] = 6 M), referred to as *concentrated HCl* in the following;
- HCl (37 %) : H_2O = 1 : 10 ([HCl] = 1.2 M), referred to as *diluted HCl* in the following.

While the use of concentrated and diluted HCl was proven to be efficient for the removal of oxides without inducing any damage on InGaAs surfaces, the preparation of InP appears to be more delicate [52-56]. As a consequence, a particular focus was put on the wet preparation of these surfaces to determine whether or not the above listed wet solutions are adapted. To do so, InP samples were dipped in the two solutions and the surfaces' roughnesses were measured thanks to an AFM characterization (Figure 2.18).

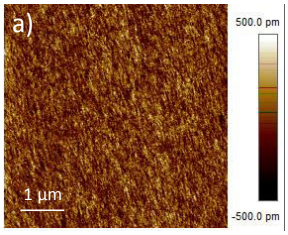
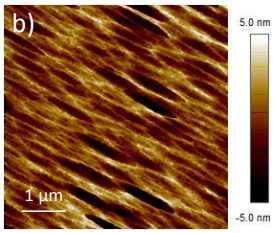
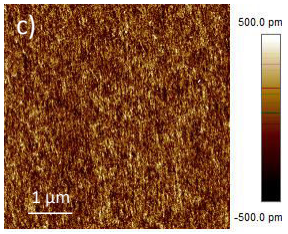
Reference	HCl :H_2O = 1 :2	HCl : H_2O = 1 :10
		
RMS roughness < 0.2 nm	RMS roughness = 1.7 nm	RMS roughness < 0.2 nm

Figure 2.18: AFM scans of an InP surface (a) before and after a wet surface preparation in (b) HCl:H_2O (1:2) and (c) HCl:H_2O (1:10).

As highlighted by the important roughness increase, the use of concentrated HCl severely deteriorated the InP surfaces. The appearance of the characteristic *boat-shaped* roughness was reported in several studies [52, 53]. For concentrations higher than 2 M, the HCl molecules anisotropically etch the InP as the etching rate depends on the crystalline orientation, the (111)-In planes acting as etch stop. As a consequence, the concentrated HCl is not adapted to the wet surface preparation of InP surfaces

Eventually, diluted HCl being efficient and nondestructive on both InP and InGaAs, it was selected for the pre metallization wet surface preparation of the III-V.

Plasma treatment

Because the wet preparation of the surfaces and the deposition of the metallization are carried out in different equipments, an oxide regrowth always occurs. Obviously the latter is very harmful for the formation of ohmic contacts as it would significantly increase the specific contact resistivity and might inhibit the solid state reactions in the case of intermetallic compounds formation (see next section). To remedy this, an additional surface preparation which consists in a plasma treatment is made in the deposition tool. Various plasma are available in the CEA-LETI clean room and were tested in our group [56-58]. In these studies, the beneficial effect of Ar or He plasma treatments on InGaAs surfaces is reported. Both of them allow an efficient removal of native oxides without damaging the InGaAs surface morphology and composition. However, the preparation of InP surfaces is more delicate as Ar preclean removes efficiently the oxides present on such surfaces but modifies their crystallinity and stoichiometry (see section 3.4.2) [56, 59]. Similar trends can be found in the literature were it is explained that the Ar^+ ions firstly stretch the In-P atomic bonds before breaking them [60-62]. Similar studies were carried out with He plasma preclean processes. The latter remove efficiently the oxides while having a lower impact on the InP surfaces [56]. However, while the Ar preclean is very common, the He one is rarer in the deposition equipments. As a consequence, while the use of the He preclean seems to be a more adapted compromise for the preparation of III-V surfaces, we were bound to use the Ar preclean in our first experiments.

2.6.2 CMOS-compatible metallization

In the frame of silicon photonics, the formation of ohmic contacts relies not only on the absence of oxides on the semiconductor surface, but also on the integration of Si-compatible materials. To do so, after the two-step surface preparation described above, the wafers are transferred in a deposition chamber. As explained in the introduction of section 2.6, the metal in contact with the semiconductor (*i.e.* the metallization) is differentiated from the filling metal (*i.e.* the plug) in this

innovative integration scheme. This choice allows a more precise tuning of the metal / semiconductor interface as the nature of the layer covering the InP and InGaAs surfaces is crucial for the formation of ohmic contacts with low contact resistivity (ρ_C). In this respect, the integration of the metallization can be achieved thanks to two strategies:

- One can choose to deposit directly the metal(s) or the intermetallic compound(s) of interest on the III-V surface. The stabilization of the phase(s) is achieved by mean of an annealing process.
- One can also choose to deposit a metal and to perform a thermal treatment for the purpose of forming one or several intermetallic compound(s) at the interface by solid state reaction with the III-V.

Each phase that is deposited or that arises from the solid state reactions offers various electrical properties (resistivity, work function, Schottky barrier height, interface and gap defects…) and thermo-kinetic properties (dopant and/or element distribution, growth kinetics, thermal stability, texture…). As a consequence, the identification of the phase formation sequence, of the driving forces and finally of the existing range of each arising compound is key to form stable and reproducible ohmic contacts. The nature of the metal that is deposited must be carefully chosen to form ohmic contacts on n-InP and p-InGaAs surfaces while being available in a front-end silicon microelectronics environment. In this respect, Ti which is a very common metal such an environment was firstly selected. Indeed, the Ti-based contacts reported in Table 1.2 and Table 1.3 give access to ohmic contacts with low specific contact resistivities on n-InP and p-InGaAs. Similarly, based on Table 1.2, the Ni-based metallizations were considered as potential candidates. More precisely, the Ni-Au-Ge-based contacts exhibit interesting electrical behavior with specific contact resistivities as low as 1.3×10^{-7} Ω.cm². It has been suggested by several groups that Au and Ge only play a minor role in the performances of these contacts while the presence of Ni might be determining [63-65].

Although the primary selection of the metal was made based on literature, extensive studies were then carried out on n-InP and p-InGaAs. In order to identify the metallurgical properties of metal / semiconductor systems along with the driving forces responsible for the formation of the observed intermetallic compounds, metallurgical studies were conducted (see chapter 3). The identification of the available levers for the lowering of the contact resistance will be presented tanks to the theory of conduction modes in metal/semiconductors systems in chapter 4. The latter will also be dedicated to the electrical characterizations of the contacts over a wide range of annealing temperatures. Finally, by crossing these studies, we will be able to select the most accurate metallization(s) and process window(s) for the formation of Si-compatible ohmic contacts both on n-InP and p-InGaAs.

2.7 Metallization encapsulation and Plug integration

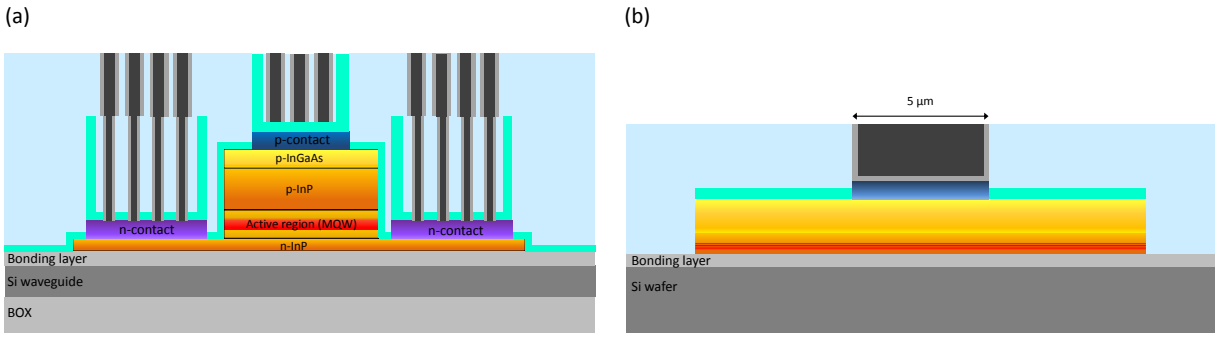


Figure 2.19: Schematic representation of the integrated contact metallization and plug contacts (a) on the III-V laser and (b) (b) on the morphological test structures.

In order to electrically connect the metallizations that are located at the bottom of the contact cavities, plugs must be integrated. The planar integration of these plugs is enabled thanks to a damascene CMP[3]. This process is highly dependent on the density and dimensions of the plugs. A too high density would lead to a metal over polishing due to an erosion phenomenon; too important dimensions (> 5 - 10 µm) would lead to an important mechanical metal over polishing called dishing [66]. Thus, on the laser while the metallization is deposited in contact cavities that measure 40 µm x 500 µm on n-InP and 5 µm x 500 µm on p-InGaAs, the plug integration requires smaller cavities. To enable such a dual integration, after its deposition, the metallization is encapsulated by a dielectric stack. The layer deposited in the first place will be used as an etch stop and is composed of the conformal SiN deposited at 300 °C. Because this dielectric stack is located close to the active region of the laser, it must present the same optical and thermal characteristics as the laser's encapsulation. Moreover, the chosen dielectric must be easily planarized after its deposition, leading to the choice of SiO_2 for the encapsulation of the metallizations. A hard mask composed of the conformal SiN can finally be deposited on top of this stack. Subsequently to the dielectric stack deposition, cavities measuring a few micrometers squared are opened down to the SiN ecth stop layer and then down to the metallization.

The filling of the contact cavities can be realized thanks to various metals, such as Cu, Al and W. However, it must meet several requirements in terms of integration and electrical properties:

- The filling metal must present a low resistivity (< 10.10^{-6} Ω.cm);
- The nucleation of the filling metal must be possible in small cavities (from 1 µm);

[3] Damascene CMP was firstly developed to electrically isolate Cu interconnect plugs because of the difficulty to pattern this material thanks to conventional etching techniques [70].

- The filling metal must be compatible with a chemical-mechanical polishing which excludes the noble metals;
- The related deposition and polishing processes must be known and available.

Based on these criteria, it appears that the Al would not be suitable as its polishing is highly challenging. This kind of metal is therefore used in non-planar steps, which excludes a damascene integration. The Al also presents some issues related to the non-negligible electromigration that occurs when a current flows through it [67]. Concerning Cu, while it is widely used in metallic lines, it is not the most adapted for vias. Indeed, the Cu is known to strongly diffuse thought the underlying metallization and into the semiconductor, therefore inducting strong degradations of the interfacial region [68]. Finally, the Cu does not answer the requirements of middle-end of line (MEOL)[4] in terms of contamination and is thus dedicated to back-end of line (BEOL)[2] integration steps. Therefore, the filling metal that was ultimately retained in our integration is a W deposited by CVD. The precursor that is used for its deposition is composed of WF_6 leading to the presence of some F in the plugs. Moreover, the W requires a seed layer to enable its nucleation. As a consequence, a seed layer also acting as diffusion barrier to F must be deposited on the walls of the cavities before the filling metal. Usually, it is composed of Ti / TiN deposited by CVD as displayed in Figure 2.20.

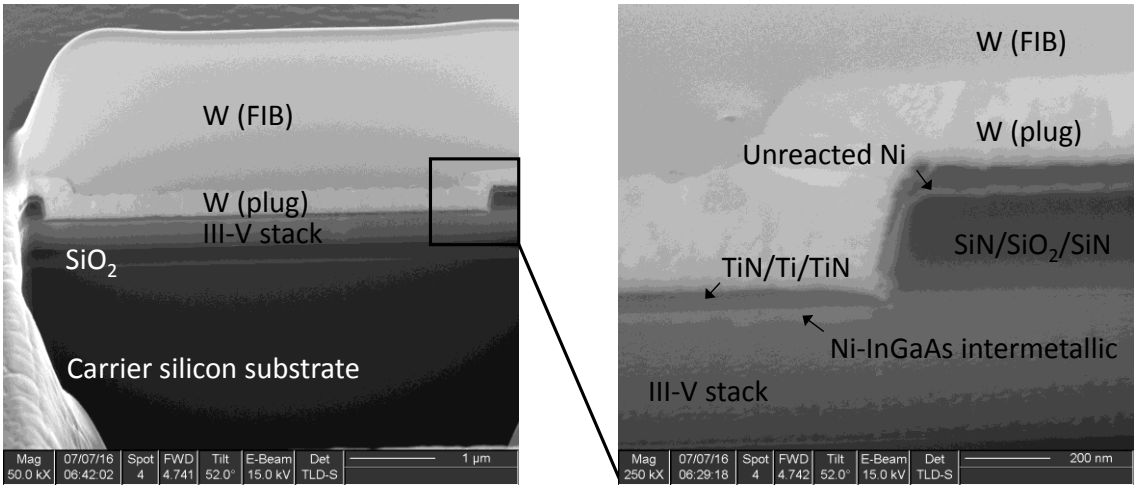


Figure 2.20: FIB/SEM image of a contact cavity on InGaAs displaying the Ni-InGaAs intermetallic compound encapsulated by a TiN layer, the classical Ti/TiN diffusion barrier and the W plug filling before the damascene CMP. Note that the morphological test structures' contact cavities measure 5 µm x 5 µm and that the plug was therefore directly deposited on the metallization.

An innovative alternative to TiN is currently being developed within the framework of collaboration with Applied Materials: the F-less W liner [69]. While the latter is not yet fully mature, the electrical

[4] The front-end-of-line (FEOL) is the first portion of the integrated circuit fabrication where the individual devices are patterned in the semiconductor. The middle end of line (MEOL) then covers the steps dedicated to the metallization and plug integration. Finally, the back end of line (BEOL) corresponds to the interconnection of the individual devices with wiring on the wafer.

properties of both available liners were probed. To do so, thin layers of TiN and F-less W liners were deposited on oxidized Si wafers and the corresponding resistivities were measured. The corresponding results are plotted as a function of the films thicknesses in Figure 2.21. It appears that the F-less W resistivity is at least two times less important than that of the classical TiN liner which opens the way for lowering the plug resistivity and therefore to a minimization of the overall resistance.

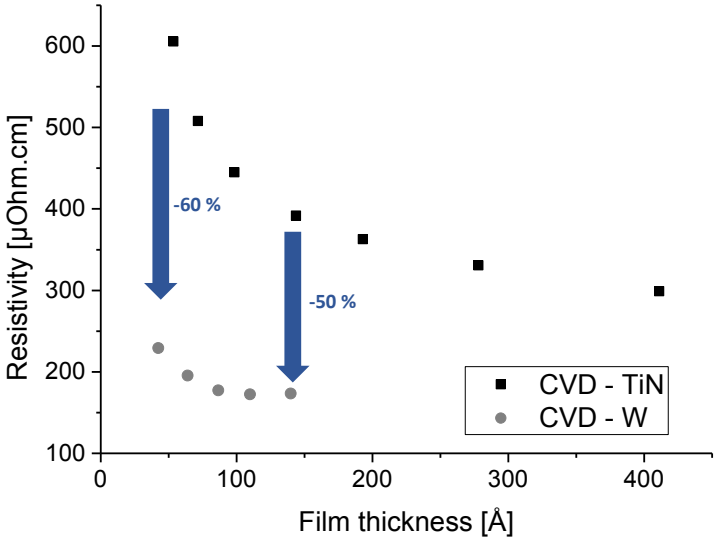


Figure 2.21: Resistivity of CVD-TiN and CVD F-less W as a function of the films thicknesses.

Finally, thanks to the planar nature of these structures, an additional metal level can be integrated on top of the contact cavities. This level can be used in electrical test structures as a probing layer or on the actual devices as an interconnection level. Generally speaking, it is composed of a diffusion barrier and of a filling metal which are respectively composed of Ti/TiN and AlCu in the case of the present integration. The resulting structure is presented in cross section in Figure 2.22.

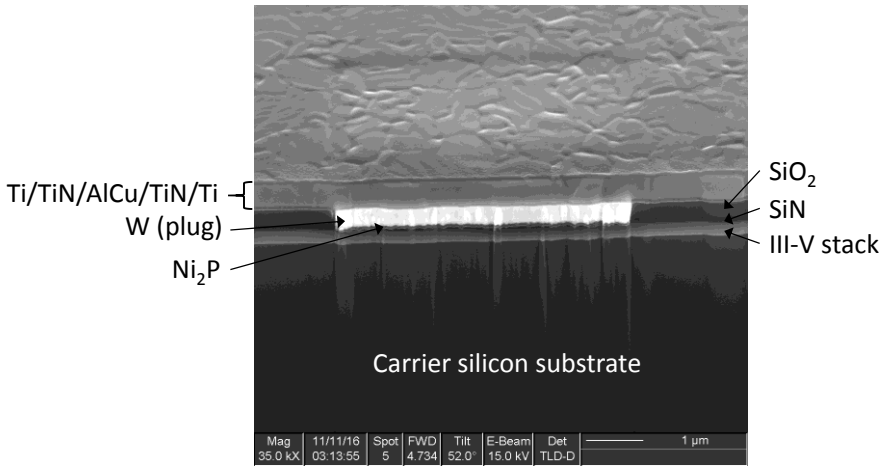
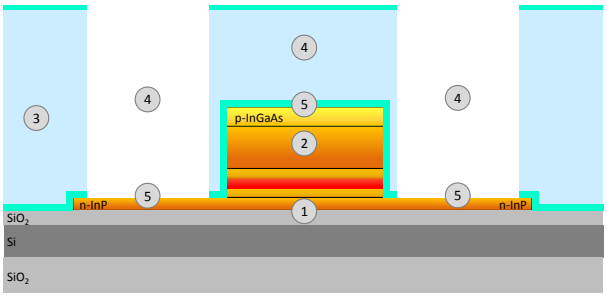


Figure 2.22: FIB/SEM cross section of a fully integrated Ni_2P-based contact on n-InP. Note that the morphological test structures' contact cavities measure 5 µm x 5 µm and that the plug was therefore directly deposited on the metallization.

2.8 Conclusion

In this chapter we addressed the problematic of contacts' integration to III-V surfaces in the frame of Silicon Photonics. Taking into account the restrictions linked to a functioning laser device and that of a Si-compatible enforcement, new contacts' compositions and integration scheme were proposed as summarized in Figure 2.23. Thanks to morphological, compositional and optical characterizations we were able to optimize the contacts' integration scheme while minimizing the optical losses of the laser device. By doing so, we were also able to propose potential solutions to further improve this integration scheme in the future. In the following chapters, particular focus will be put on the metallurgical study of the contact metallization and on the electrical study of the integrated contacts. Combining these studies, we will be able to provide further insight concerning the effect of the dielectric encapsulation and of the metallization (metal + subsequent thermal budget) on the electrical characteristics of the contacts and on their thermal stability.



1 – Bonding of the III-V on the Si substrate

Direct bonding of the III-V laser on oxidized SOI wafer

2 – Etching of the III-V

SiN hard mask composed of conformal SiN deposited at 300 °C (upgrade = Low stress SiN deposited at 300 °C)

ICP plasma etching

3 – Dielectric encapsulation

SiN and SiO_2 deposited by PE-CVD at 300 °C

Planarization of the dielectric stack by CMP

4 – Etching of the contact cavities

SiN hard mask composed of conformal SiN deposited at 300 °C (upgrade = Low stress SiN deposited at 300 °C)

Dry etching of the dielectric stack (SiO_2 + majority of SiN) thanks to a CH_2F_2 plasma

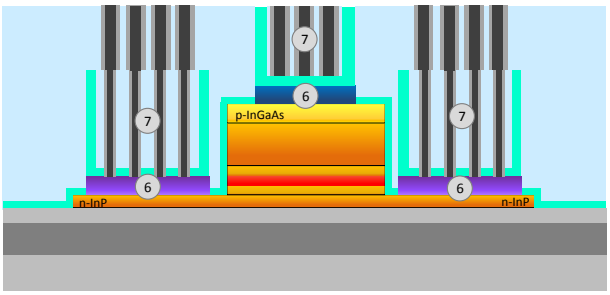
Finalization of the SiN etching thanks to diluted HF

5 – Surface preparation

Combination of diluted HCl : H_2O (1 : 10; [HCl] = 1.2 M) and in situ He pre clean

6 – CMOS-compatible metallization

Deposition of Ni or Ti and thermal treatment to stabilize the deposited phases or to form intermetallic compound(s) (electrical and metallurgical studies in chapters 3 and 4)



7- Encapsulation of the metallization

SiN and SiO_2 deposited by PE-CVD at 300 °C

Planarization of the dielectric stack by CMP

7 – Plugs

Dry etching of the dielectric stack (SiO_2 + SiN) thanks to a CH_2F_2 plasma

Ti/TiN liner (upgrade = F-less W liner) and W fill

Figure 2.23: Summary of the developed steps for the integration of Si-microelectronics compatible contacts on a III-V laser in the framework of Silicon Photonics.

CHAPTER 2 - Bibliographic references

[1] E. Ghegin, Ph. Rodriguez, F. Nemouchi, C. Jany, M. Brihoum, A. Halimaoui, I. Sagnes, and B. Szelag. Towards contact integration for III-V/Silicon heterogeneous photonics devices. *2016 IEEE International Interconnect Conference, 2016 Advanced Metallization Conference (IITC/AMC)*, 2016.

[2] M. Rosenzweig, M. Mohrle, H. Duser, and H. Venghaus. Threshold-current analysis of InGaAs-InGaAsP multiquantum well separate-confinement lasers. *IEEE Journal of Quantum Electronics*, 27(6):1804–1811, Jun 1991.

[3] L.A. Coldren and S.W. Corzine. *Diode lasers and photonic integrated circuits*. Wiley series in microwave and optical engineering. Wiley, 1995.

[4] J. Piprek. *Semiconductor Optoelectronic Devices, Introduction to Physics and Simulation*. 2003.

[5] T. Takagi. Refractive index of $Ga_{1-x}In_xAs$ prepared by vapor-phase epitaxy. *Japanese Journal of Applied Physics*, 17(10):1813, 1978.

[6] Batop optoelectronic, 2016.

[7] B. Broberg and S. Lindgren. Refractive index of $In_{1-x}Ga_xAs_yP_{1-y}$ layers and InP in the transparent wavelength region. *Journal of Applied Physics*, 55(9):3376–3381, 1984.

[8] G. D. Pettit and W. J. Turner. Refractive index of InP. *Journal of Applied Physics*, 36(6):2081–2081, 1965.

[9] Y.P. Varshni. Temperature dependence of the energy gap in semiconductors. *Physica*, 34(1):149 – 154, 1967.

[10] S. Paul, J. B. Roy, and P. K. Basu. Empirical expressions for the alloy composition and temperature dependence of the band gap and intrinsic carrier density in $Ga_xIn_{1-x}As$. *Journal of Applied Physics*, 69(2):827–829, 1991.

[11] N. K. Dutta and R. J. Nelson. Temperature dependence of threshold of InGaAsP/InP double-heterostructure lasers and auger recombination. *Applied Physics Letters*, 38(6):407–409, 1981.

[12] J. Piprek. Advanced analysis of high-temperature failure mechanisms in telecom lasers. *Proceedings SPIE*, 4533:70–81, 2001.

[13] Isp optics.

[14] Refractive index . info, 2008-2016.

[15] R. Kitamura, L. Pilon, and M. Jonasz. Optical constants of silica glass from extreme ultraviolet to far infrared at near room temperature. *Applied Optics*, 46(33):8118–8133, Nov 2007.

[16] S.-M. Lee, David G. Cahill, and Thomas H. Allen. Thermal conductivity of sputtered oxide films. *Physical Review B: Condensed Matter and Materials Physics*, 52:253–257, Jul 1995.

[17] Globalkyocera.com.

[18] Azo materials.

[19] P. Auerkari. *Mechanical and Physical Properties of Engineering Alumina Ceramics*. Technical Research Centre of Finland, 1996.

[20] Hiroyuki Fujiwara. *Spectroscopic Ellipsometry: Principles and applicationS*. John Wiley & Sons, Ltd, 2007.

[21] B. Castellon. L'ellipsométrie spectroscopique. *SOPRA - les fondamentaux*.

[22] N-E. Ghellai, N. Benmansour, and A. Chabane Sari. Ellipsométrie spectroscopique. *Photoniques*, (51):22–27, February 2011.

[23] Horiba Jobin Yvon. TN11: Tauc-Lorentz dispertion formula. *Horiba technical note*, 2006.

[24] R. Beigelbeck, F. Kohl, F. Keplinger, J. Kuntner, and B. Jakoby. A novel characterization method for thermal thin-film properties applied to PECVD silicon nitride. In *Sensors, 2007 IEEE*, pages 938–941, Oct 2007.

[25] M. von Arx, O. Paul, and H. Baltes. Process-dependent thin-film thermal conductivities for thermal cmos mems. *Journal of Microelectromechanical Systems*, 9(1):136–145, March 2000.

[26] P. Eriksson, J. Y. Andersson, and G. Stemme. Thermal characterization of surface-micromachined silicon nitride membranes for thermal infrared detectors. *Journal of Microelectromechanical Systems*, 6(1):55–61, Mar 1997.

[27] Kohl F Jakoby B. Kuntner J, Jachimowicz A. Determining the thin-film thermal conductivity of low temperature PECVD silicon nitride. In *Proc. Eurosensors XX*, 2006.

[28] C. E. Raudzis, F. Schatz, and D. Wharam. Extending the 3Ï? method for thin-film analysis to high frequencies. *Journal of Applied Physics*, 93(10):6050–6055, 2003.

[29] F.R. Brotzen, P.J. Loos, and D.P. Brady. Thermal conductivity of thin SiO2 films. *Thin Solid Films*, 207(1):197 – 201, 1992.

[30] David G. Cahill and Thomas H. Allen. Thermal conductivity of sputtered and evaporated SiO2 and TiO2 optical coatings. *Applied Physics Letters*, 65(3):309–311, 1994.

[31] David G. Cahill. Heat transport in dielectric thin films and at solid-solid interfaces. *Microscale Thermophysical Engineering*, 1:85–109, 1997.

[32] S Callard, G Tallarida, A Borghesi, and L Zanotti. Thermal conductivity of SiO2 films by scanning thermal microscopy. *Journal of Non-Crystalline Solids*, 245(1â??3):203 – 209, 1999.

[33] Heng-Chieh Chien, Da-Jeng Yao, Mei-Jiau Huang, and Tien-Yao Chang. Thermal conductivity measurement and interface thermal resistance estimation using SiO2 thin film. *Review of Scientific Instruments*, 79(5), 2008.

[34] O. W. Kading, H. Skurk, and K. E. Goodson. Thermal conduction in metallized silicon dioxide layers on silicon. *Applied Physics Letters*, 65(13):1629–1631, 1994.

[35] M. B. Kleiner, S. A. Kuhn, and W. Weber. Thermal conductivity measurements of thin silicon dioxide films in integrated circuits. *IEEE Transactions on Electron Devices*, 43(9):1602–1609, Sep 1996.

[36] L. Tranchant, J. Ordonez-Miranda, T. Matsumoto, S. Gluchko, T. Antoni, S. Volz, and K. Miyazaki. Measurement of the in-plane thermal conductivity of SiO2 thin films due to surface phonon-polaritons. In *Thermal Investigations of ICs and Systems (THERMINIC), 2015 21st International Workshop on*, pages 1–5, Sept 2015.

[37] Tsuneyuki Yamane, Naoto Nagai, Shin-ichiro Katayama, and Minoru Todoki. Measurement of thermal conductivity of silicon dioxide thin films using a 3w method. *Journal of Applied Physics*, 91(12):9772–9776, 2002.

[38] R. M. Costescu, D. G. Cahill, F. H. Fabreguette, Z. A. Sechrist, and S. M. George. Ultra-low thermal conductivity in W/Al2O3 nanolaminates. *Science*, 303(5660):989–990, 2004.

[39] David G. Cahill, S.-M. Lee, and Torbjorn I. Selinder. Thermal conductivity of k-Al2O3 and a-Al2O3 wear-resistant coatings. *Journal of Applied Physics*, 83(11):5783–5786, 1998.

[40] S. Saji, K. Matsumoto, T. Shibayanagi, T. Yamasaki, Y. Ogino, T. Sakata, and T. Sakata. Crystallization process in amorphous Al_2O_3 and Al-Ti-O-N mixed powders prepared by mechanical alloying. *Journal of the Japan Institute of Metals*, 56:509–516, 1992.

[41] M. Rafiei, M.H. Enayati, and F. Karimzadeh. Mechanochemical synthesis of $(Fe,Ti)_3Al$ - Al_2O_3 nanocomposite. *Journal of Alloys and Compounds*, 488(1):144 – 147, 2009.

[42] V. Cimalla, M. Baeumler, L. Kirste, M. Prescher, B. Christian, T. Passow, F. Benkhelifa, F. Bernhardt, G. Eichapfel, M. Himmerlich, S. Krischok, and J. Pezoldt. Densification of thin aluminum oxide films by thermal treatments. *Materials Sciences and Applications*, 5:628–638, 2014.

[43] T. Maruyama, N. Fujiwara, K. Siozawa, and M. Yoneda. Analysis of fluorocarbon deposition during SiO_2 etching. *Japanese Journal of Applied Physics*, 35(4S):2463, 1996.

[44] G. S. Oehrlein, R. M. Tromp, J. C. Tsang, Y. H. Lee, and E. J. Petrillo. Near-surface damage and contamination after CF_4/H_2 reactive ion etching of Si. *Journal of The Electrochemical Society*, 132(6):1441–1447, 1985.

[45] Y. Wang, S. W. Graham, L. Chan, and S. Loong. Understanding of via etch-induced polymer formation and its removal. *Journal of The Electrochemical Society*, 144(4):1522–1528, 1997.

[46] J. Wang, J. Tian, B. Xiong, C. Sun, Z. Hao, and Y. Luo. Deep InP gratings for opto-electronic devices etched by $Cl_2/CH_4/Ar$ inductively coupled plasma. *Chinese Physics Letters*, 23:2158–2160, 2006.

[47] F. Rodrigues De Almeida, R.K. Yamamoto, and H.S. Maciel. Reactive ion etching of PECVD silicon nitride in SF_6 plasma. *Journal of Nuclear Materials*, 200(3):371 – 374, 1993.

[48] Yun Sun, Zhi Liu, Francisco Machuca, Piero Pianetta, and William E. Spicer. Optimized cleaning method for producing device quality inp(100) surfaces. *Journal of Applied Physics*, 97(12), 2005.

[49] D.L. Rath, R. Jagannathan, K.J. McCullough, H.F. Okorn-Schmidt, K.P. Madden, and K.R. Pope. Process for removing etching residues, etching mask and silicon nitride and/or silicon dioxide, March 7 2000. US Patent 6,033,996.

[50] F.L. Lie, W. Rachmady, and A.J. Muscat. In0.53ga0.47as(1 0 0) native oxide removal by liquid and gas phase hf/h2o chemistries. *Microelectronic Engineering*, 87(9):1656 – 1660, 2010. 11th {SEMATECH} Surface Preparation and Cleaning Conference.

[51] Daitetsu Kikuchi and Sadao Adachi. Chemically cleaned InP(100) surfaces in aqueous HF solutions. *Materials Science and Engineering: B*, 76(2):133–138, July 2000.

[52] D. Cuypers, S. De Gendt, S. Arnauts, K. Paulussen, and D. H. van Dorp. Wet chemical etching of InP for cleaning applications: I. An oxide formation/oxide dissolution model. *ECS Journal of Solid State Science and Technology*, 2(4):P185–P189, 2013.

[53] D. H. van Dorp, D. Cuypers, S. Arnauts, A. Moussa, L. Rodriguez, and S. De Gendt. Wet chemical etching of InP for cleaning applications: II. Oxide removal. *ECS Journal of Solid State Science and Technology*, 2(4):P190–P194, 2013.

[54] D. Cuypers, D. H. van Dorp, M. Tallarida, S. Brizzi, T. Conard, L. N. J. Rodriguez, M. Mees, S. Arnauts, D. Schmeisser, C. Adelmann, and S. De Gendt. Study of InP surfaces after wet chemical treatments. *ECS Journal of Solid State Science and Technology*, 3(1):N3016–N3022, 2014.

[55] D. H. van Dorp, S. Arnauts, D. Cuypers, J. Rip, F. Holsteyns, S. De Gendt, and J. Kelly. Nanoscale etching of $In_{0.53}Ga_{0.47}As$ in H_2O_2/HCl solutions for advanced CMOS processing. *ECS Journal of Solid State Science and Technology*, 3(6):P179–P184, 2014.

[56] Ph. Rodriguez, L. Toselli, E. Ghegin, M. Rebaud, N. Rochat, N. Chevalier, E. Martinez, and F. Nemouchi. Cleaning of InGaAs and InP layers for Nanoelectronics and Photonics contact technology applications. *ECS Transactions*, 69(8):251–259, 2015.

[57] Ph. Rodriguez, L. Toselli, E. Ghegin, N. Rochat, N. Chevalier, E. Martinez, and F. Nemouchi. Ingaas surface pretreatment prior to metal solid-state reactions for low resistance contacts. In *2015 15th International Workshop on Junction Technology (IWJT)*, pages 54–57, June 2015.

[58] Ph. Rodriguez, L. Toselli, E. Ghegin, N. Chevalier, N. Rochat, E. Martinez, and F. Nemouchi. In situ cleaning of InGaAs surfaces prior to low contact resistance metallization. *Microelectronic Engineering*, 156:91 – 96, 2016.

[59] E. Ghegin, F. Nemouchi, J. Labar, C. Perrin, K. Hoummada, S. Favier, S. Gurban, and I. Sagnes. Phase formation in the Ni/InP contacts for heterogeneous III/V-Silicon-Silicon photonic integration. *Microelectronic Engineering*, 156:86 – 90, 2016.

[60] P.S. Mangat, P. Soukiassian, Y. Huttel, Z. Hurych, B. Gruzza, and A. Porte. Low energy Ar^+ ion bombardment induced modification of surface atomic bond lengths on InP(100) wafer. *Applied Physics Letters*, 63(14):1957–1959, Oct 1993.

[61] Q. Zhao, Z. W. Deng, R. W. M. Kwok, and W. M. Lau. Damage of InP (110) induced by low energy Ar^+ and He^+ bombardment. *Journal of Vacuum Science & Technology A*, 18(5):2271–2276, 2000.

[62] J-Y. Hu, W. Mahmood, and Q. Zhao. Effect of Ar^+, He^+, and S^+ irradiation on n-InP single crystal. *Chinese Journal of Chemical Physics*, 27(1):82–86, 2014.

[63] M. F. O'Keefe, R. E. Miles, and M. J. Howes. Nickel in ohmic contacts to indium phosphide. *Proceedings SPIE*, 1144:361–367, 1989.

[64] RJ Graham and JW Steeds. Microstructural investigation of large area and device size AuGeNi contacts on InP. *INSTITUTE OF PHYSICS CONFERENCE SERIES*, 67:507–512, 1983.

[65] J. Morais, T. A. Fazan, R. Landers, and E. A. S. Sato. Ohmic contacts formation on n-inp. *Journal of Applied Physics*, 79(9):7058–7061, 1996.

[66] Z. Stavreva, D. Zeidler, M. Plotner, and K. Drescher. Chemical mechanical polishing of copper for multilevel metallization. *Applied Surface Science*, 91(1):192 – 196, 1995.

[67] H. Mori, H. Okabayashi, and M. Komatsu. Electromigration in layered al lines studied by in-situ ultra-high voltage electron microscopy. *Thin Solid Films*, 300(1):25 – 29, 1997.

[68] S.P. Murarka, R.J. Gutmann, A.E. Kaloyeros, and W.A. Lanford. Advanced multilayer metallization schemes with copper as interconnection metal. *Thin Solid Films*, 236(1):257 – 266, 1993.

[69] J. Bakke, Yu Lei, Yi Xu, K. Daito, Xinyu Fu, Guoqiang Jian, Kai Wu, Raymond Hung, R. Jakkaraju, and N. Breil. Fluorine-free tungsten films as low resistance liners for tungsten fill applications. In *2016 IEEE International Interconnect Technology Conference / Advanced Metallization Conference (IITC/AMC)*, pages 108–110, May 2016.

[70] R. V. Joshi. A new damascene structure for submicrometer interconnect wiring. *IEEE Electron Device Letters*, 14(3):129–132, March 1993.

CHAPTER 3

METALLURGICAL STUDIES OF SI-COMPATIBLE METALLIZATIONS ON n-InP AND p-InGaAs

Outline

The formation of ohmic contacts with low specific resistivity is the key to form efficient and reliable electronic and photonic devices. The light source of a Silicon Photonics circuit, *i.e.* the laser, is not an exception to this rule. In the previous chapter, we mentioned the advantage of performing thermal treatments after the metal deposition. Indeed, the latter can either stabilize the deposited phases or lead to the formation of intermetallic compounds at the interface between the metal and the semiconductor. In any case, it is of great importance to characterize the morphology and the composition of the annealed systems. Forming low resistance, stable and reproducible contacts requires the identification of the phase sequences and the existing range of each phase in terms of thermal budget. In this chapter we will present metallurgical studies that were carried out for this purpose. After an introduction to the formation of intermetallic compounds in the case of thin films, we will present the research conducted on the Ni-based metallizations and the results obtained with Ti-based metallizations.

3.1 Formation of intermetallic compounds in the case of thin films

Intermetallic compounds have been widely studied and used on Si-based devices over the past decades [1-8]. The so-called silicidation process allows the formation of low resistance contacts that are also thermally stable. Rapidly, the formation of intermetallic compounds has been transferred on III-V semiconductors such as GaAs, InGaAs and InP to take advantage of its numerous benefits [9-29]. Regardless of the semiconductor's nature, the formation of such contacts relies on four main steps. The solid-state reactions being very sensitive to oxides or contaminants, the semiconductor surfaces are firstly cleaned in a wet solution, rinsed in deionized water and blown dry. The wafers are immediately transferred in a deposition tool were a plasma pre-clean removes all oxides that could have regrown during their transfer. These precautions are essential to ensure the repeatability of the intermetallic compounds' formation. The metal is deposited on the semiconductor at room temperature or at higher temperature ($T < 150$ °C). Finally, an annealing process is conducted, either in a traditional furnace or by rapid thermal annealing (RTA) to form the intermetallic compounds. This thermal treatment is generally performed under low background concentration of oxygen to limit the oxidation of the metal and of the interface during the intermetallic formation (see section 3.1.4). Because every semiconductor reacts differently to these steps, the latter are adapted to optimize the final integrated contact, *i.e.,* to meet the requisites randomly listed below [8].

Table 3.1: Requisites linked to the use of intermetallic compounds on semiconductors [8]

1. Low resistivity	8. Oxidation resistance
2. Good adhesion to semiconductor	9. Good adhesion to and minimal reaction with the surrounding materials (other than the semiconductor)
3. Low contact resistance to semiconductor	10. Low stress
4. Appropriate Schottky barrier height or ohmic behavior with heavily doped semiconductor (n^+ or p^+) over the targeted range of polarization	11. Compatibility with other processing steps such as lithography and etching
5. Thermal stability	12. Minimizing metal diffusion
6. Appropriate morphology for subsequent lithography and etching processes	13. High electromigration resistance
7. High corrosion resistance	14. Formability at low temperature

Generally speaking, the formation of intermetallic compounds can rely on different driving forces and can be sensitive to the presence of defects and impurities. The next sections will be dedicated to the presentation of these mechanisms and will therefore give relevant insights for the integration of the Si front-end compatible metallization.

3.1.1 Formation of intermetallic compounds - Generalities

When two materials, called A and B, are put in contact, a sharp A/B interface is created. Generally speaking, this kind of system is not thermodynamically stable and will therefore evolve towards a less energetic state. Most of the time, this evolution is enabled by the supply of external energy, *i.e.* thermal budget, stress or polarization for example, and is always well described by the A/B equilibrium phase diagram. This reactive diffusion theory was firstly proposed by Gas and d'Heurle and Zhang and d'Heurle [1, 30].

The evolution of this A-B system can strongly differ, depending on the initial compounds miscibility. If A and B are totally miscible, the system evolves toward the formation of a solid solution between A and B ranging from pure A to pure B and displaying a unique crystallographic structure. If the system tends to a demixion, two solid solutions (A-rich and B-rich) appear at the A/B interface which

becomes a A(B) / B(A) interface. Most cases lie somewhere in between these two extrema and N intermediate phases described by the equilibrium diagram coexist between A and B at a given temperature. The unique A/B interface is thus replaced by N+1 interfaces as illustrated in Figure 3.1. These evolutions and the temperature at which they occur strongly depend on the thickness of the layers; a system composed of "thin" films (~ 100 nm) generally presents a rapid kinetics of formation compared to the corresponding bulk system. Some phases that were described as stable in the bulk system might also not appear in thin films. In any cases, the reactive diffusion theory well describes the appearance of new phases / intermetallic compounds.

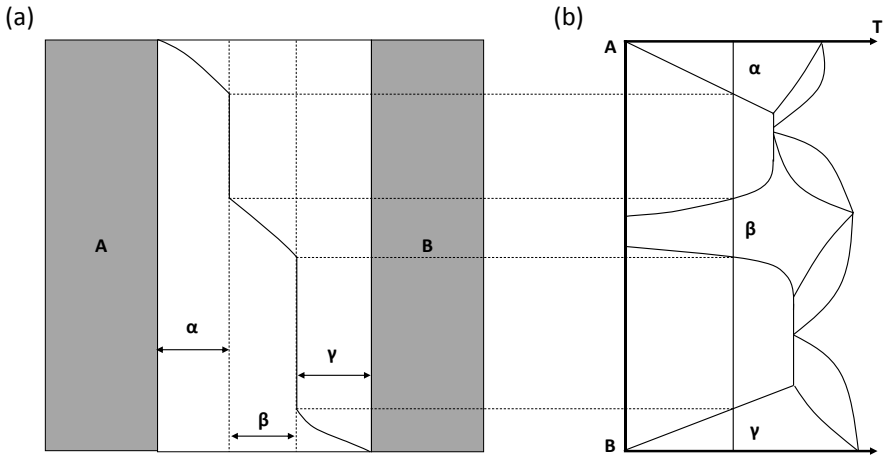


Figure 3.1: Schematic representation of (a) an hypothetic diffusion profile corresponding to the element A in a A/B diffusion couple submitted to a thermal treatment and (b) of the corresponding binary A-B equilibrium phase diagram.

3.1.2 Thin films reactive diffusion

Growth of a single phase

Let's consider a system composed of two materials, A and B, which undergoes a thermal treatment. The growth of a new phase, noted A_xB_y, between A and B requires three steps:

- The formation of a new interface;
- The diffusion of A (and/or B) through the new interface;
- The chemical reaction between A and B at the interfaces (A/A_xB_y and/or A_xB_y/B) leading to the formation of the intermediate compound: $x.A + y.B \rightarrow A_xB_y$.

In the early stages of the reaction, the thickness of the intermediate compound is small and both A and B are available at the interfaces. The growth of the compound A_xB_y is therefore only limited by the rate at which the reaction between A and B can occur. In this case, the thickness of the new phase, L, increases linearly with time (t):

$$L(t) = K_r.t$$ **Equation 3.1**

Where K_r [cm.s^{-1}] is a constant characteristic of reactions that occur at the interface.

When the intermetallic compound grows, its thickness increases. Therefore, the path that the various species have to travel before reaching the interfaces becomes more important. At some point, the growth of the new phase(s) is no more limited by the interfacial reactions but by the flux of atoms that reach the interface. The evolution of the interfacial product thickness does not vary linearly with time anymore but according to the following expression:

$$L(t) = \sqrt{K_d.t}$$ **Equation 3.2**

Where K_d $[cm^2.s^{-1}]$ is related to the diffusivity of the dominant moving species involved in the reaction.

The concatenation of this two regimes results in the "linear parabolic growth" which is well represented by the formation of silicon dioxide [31], [32]. It was demonstrated for the first time in 2005 that the sequential growth of the Ni_2Si and NiSi silicides are ruled by this law as well [33]. The change of regime occurs when the limit thickness $L_{1/2}$ is reached.

$$L_{1/2} = {K_d}/{K_r}$$ **Equation 3.3**

Simultaneous growth of several phases

When two or more phases grow simultaneously, this simple vision is slightly modified. Each compound's growth is determined by the interface reactions and diffusion coefficient of this particular phase, but also of the other phases that are present in the system. For example, let's consider a hypothetical A/B system where two phases AB and A_2B grow simultaneously and where A is the only mobile species in both phases (Figure 3.2). In these conditions, the A_2B phase can only grow at the A_2B/AB interface (A + AB → A_2B) while the AB phase can grow at both A_2B/AB (A_2B → A + AB) and AB/B interfaces (A + B → AB). By defining the fluxes in A_2B and AB respectively as J_1 and J_2, one can express the growth velocity of both phases:

$$dL_1/dt = J_1 - J_2$$
$$dL_2/dt = 2.J_2 - J_1$$ **Equation 3.4**

This couple of equations highlights the interdependence of the different phases' growth rates. As both of them can be determined by the interfacial reactions and by the diffusion of the species, one

can easily imagine the complexity of such a system. However, metal - semiconductor reactions are generally ruled by two different mechanisms and can therefore easily be divided into two categories: the diffusion and the nucleation controlled kinetics.

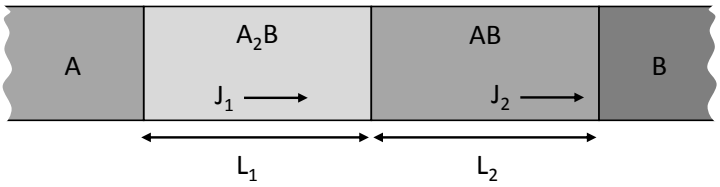


Figure 3.2: Schematic representation of the simultaneous formation of two phases by solid state reaction between two compounds (A and B), where A is the only diffusing species.

3.1.3 Kinetics of phase(s) formation

Diffusion controlled kinetics

The diffusion controlled kinetics occurs when the formation of the phases is limited by the supply of species, *i.e.*, when the interfacial reactions occur faster than the arrival of atoms at the interface. Such a kind of kinetics is quite similar for bulk and thin films reactions, but the contribution of the grain boundaries in the latter case increases the diffusivity of the species. Plotting the square of the interfacial layer's thickness as a function of time allows analyzing the kinetics into more details. Indeed, for diffusion limited kinetics, and if the formation of the various phases is sequential, this kind of plot gives rise to a series of straight lines. Their slopes for a given temperature allow determining the rate of formation which is itself directly related to the diffusivity of the dominant diffusing species (Equation 3.2). Similarly, the Arrhenius law, which was proposed by Svante Arrhenius in 1889 can provide further insights concerning the kinetics of formation. The latter gives the dependence of the rate constant of a chemical reaction, K, on the absolute temperature T (Equation 3.5). Taking the natural logarithm of this equation gives rise to Equation 3.6 which is used in the traditional Arrhenius plots to access the activation energy for diffusion / growth, E_a.

$$K = A.e^{-E_a/RT} \qquad \textbf{Equation 3.5}$$

$$\ln(K) = \frac{-E_a}{R}.\left(\frac{1}{T}\right) + \ln(A) \qquad \textbf{Equation 3.6}$$

Nucleation controlled kinetics

Contrary to the diffusion controlled growth, the nucleation controlled kinetics requires a minimal temperature to be initiated. As explained in section 3.1.1, the formation of one or several new phase(s) requires the creation of additional interfaces. When the cost in energy related to this

process, *i.e.* the surface energy (σ), is higher than the gain in free energy due to the formation of the new products (ΔG_V), additional supply of energy is required to initiate the reaction. Therefore, high temperatures are necessary to induce the formation of the additional interfaces, *i.e.*, to nucleate the new phase(s). At this point, since the diffusion is not limiting, the formation of the new compound(s) occurs rapidly once the critical nucleation temperature is reached. The nucleation of these phases is therefore ruled by the competition between the gain in free energy (ΔG_V) and the surface energy caused by the formation of new interfaces (σ). A nucleus of radius r is characterized by a free energy by unit volume:

$$\Delta G_n = ar^3.\Delta G_V + br^2.\sigma \qquad \textbf{Equation 3.7}$$

Where a and b account for the geometrical shape of the nucleus (for example, in the case of a spherical nucleus, $a = 4/3\,.\pi$ and $b = 4.\pi$). Increasing the radius of the nucleus firstly increases the corresponding total energy because of the increase in surface energy. At some point, a critical radius is reached and the cost of surface energy is compensated by the gain in free energy as represented in Figure 3.3. Nuclei smaller than this critical grain size tend to dissolve while the other tend to grow to minimize the system's energy. The rate of nucleation is given by:

$$\rho^* = K.\exp\left(-\frac{\Delta {G_n}^*}{kT}\right).\exp(-\frac{Q}{kT}) \qquad \textbf{Equation 3.8}$$

Where K is a constant, $\Delta {G_n}^*$ is the free energy of the critical nuclei which is proportional to $1/T^2$ and Q is related to the activation energy for diffusion. Thus, the nucleation rate is proportional to $\exp(-1/T^3)$ and is therefore a process that occurs in a limited range of temperature. Below the critical temperature, no nucleation takes places; above it the nucleation of new phases is fast.

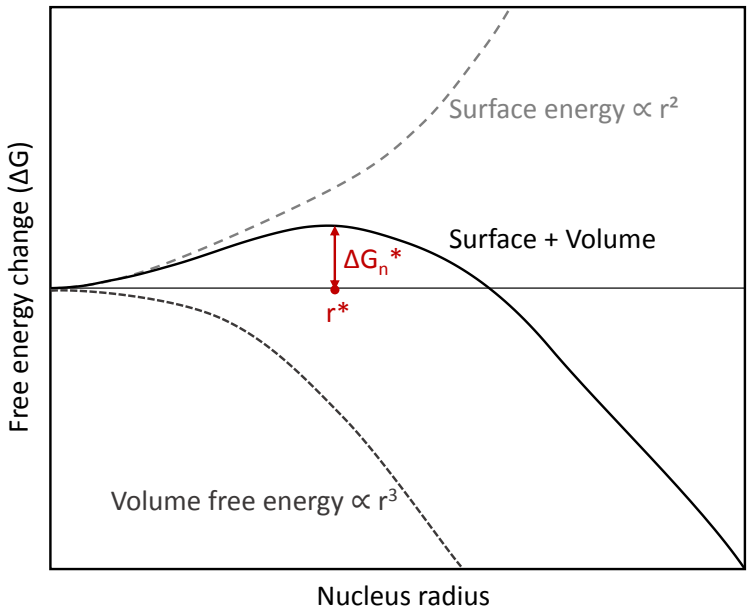


Figure 3.3: Free energy of a nucleus as a function of its radius showing the contribution of the surface, volume and their sum.

Because the nucleation limited kinetics results from a competition between the gain in free energy (ΔG_V) and the surface energy required to form new interfaces (σ), it is generally observed when the gain in free energy (ΔG_V) is small. Let's consider the hypothetical case schematized in Figure 3.4 dealing with the free energies G_V associated to a A/B system. The formation of the phase AB between A and B strongly decreases the volume free energy (ΔG_{V1}) compared to the case where A is in contact with B. Therefore, because the gain in free energy associated to this transformation is important, it will most likely compensate the energy required to form the new interfaces, namely σ. It is therefore very probable that this phase will be formed in the early stages of the reaction, even at low temperature. The free energy G_V of the system could be further minimized by forming an additional AB_x phase. However, the free energy gain associated to this transformation (ΔG_{V2}) is quite low. It might even be lower than the energy required to form new interfaces. In this case, the formation of the phase AB_x would thus be limited by the nucleation and would require the supply of external energy. As a consequence, even if the formation of the phase AB_x would enable a lowering of the overall system's energy, it might only occur at high temperatures, where the nucleation barrier is overcome.

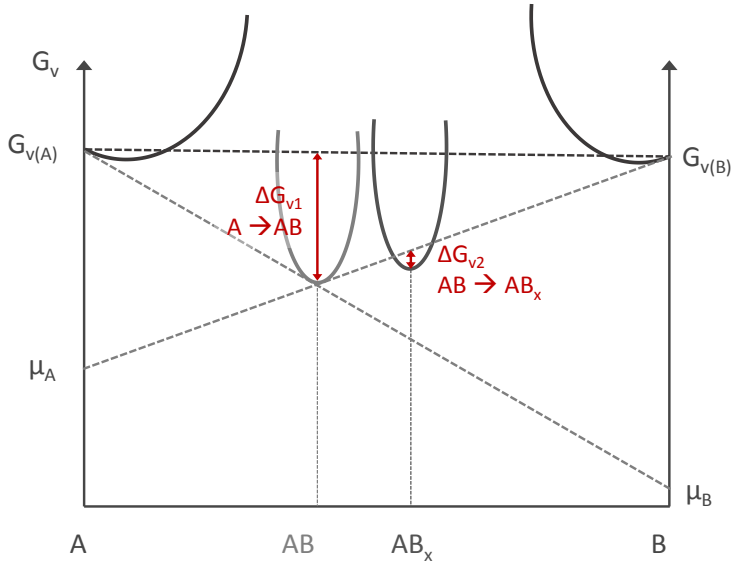


Figure 3.4: Variation of the free energy G_V associated to the formation of binary phases in a hypothetical A/B system. μ_A and μ_B correspond to the chemical potential of the compounds A and B.

It is important to note that the gap between diffusion and nucleation controlled kinetics might be small, as illustrated in section 3.4 which deals with Ni/InP intermetallic compounds. If the temperature required to initiate the nucleation is quite low, both the nucleation and the diffusion can limit the growth of the phase(s).

3.1.4 Impact of defects on intermetallic formation

In order to fully identify the mechanisms limiting or enhancing the formation of intermetallic compounds, one must additionally consider the defects and impurities that can be present on semiconductor surfaces. The effect of the latter can significantly vary depending on their nature and can therefore inhibit or enhance the formation of intermetallic compounds [34-36]. Among others, the presence of a native oxide at the surface of the semiconductor surface generally has a detrimental effect as it limits / prevents the reaction. To avoid this kind of problem, the semiconductor surfaces are always subjected to wet and/or dry preparations for the purpose of suppressing the contaminants and oxides. For example, in the integration scheme presented in Chapter 2, InGaAs and InP surfaces are always dipped in HCl solutions before undergoing Ar or He plasma treatments. On the contrary, the presence of nitrogen in the annealing ambient during the

intermetallic formation can be beneficial as it purges the systems from detrimental impurities such as oxygen [37, 38][1].

3.1.5 Thermal stability of the intermetallic compounds

Once formed, the intermetallic compounds must be stable, often over a large range of temperatures. Indeed, the processes to which the systems are subjected after the intermetallic formation might require high temperatures. It is therefore crucial to stabilize the phase(s) of interest or a least to identify the range of temperatures in which they are stable before conducting any other process. This knowledge prevents any deterioration of the stoichiometry, the morphology, and the electrical properties of the compound(s).

3.2 Experimental procedure and characterization techniques

As detailed in the previous sections, the integration of the contact metallization, *i.e.*, the metallic compound in contact with the semiconductor, relies on various mechanisms and driving forces. In the integration scheme presented in Chapter 2, two different paths were mentioned:

- The deposition of a metallic compound followed by an annealing treatment that aims to stabilize the deposited phase;
- The deposition of a metal followed by an annealing treatment for the purpose of forming one or several intermetallic compound(s) at the interface with the semiconductor.

Whatever the path chosen, we explained in the previous sections that the integration of the metallization is the key to lower the specific contact resistivity. Therefore, extensive metallurgical and morphological studies were conducted on n-InP and p-InGaAs in order to optimize the integration of the metallization on both surfaces.

3.2.1 Experimental procedure

The metallurgical and morphological studies were carried out on dedicated blanket samples. The latter are composed of 2 inches semi-insulating (001) InP substrates on top of which a 300 nm thick epitaxial layer was grown. These epitaxial layers are composed either of Si doped InP ($N_D = 3.10^{18}$ cm^{-3}) or of Zn doped InGaAs ($N_A = 3.10^{19}$ cm^{-3}). Because the presence of oxides and contaminants on the

[1] In the case of a Ti-based metallization, the nitridation of Ti during the annealing treatment can also be used to form the TiN nucleation layer and diffusion barrier for the subsequent integration of a W plug [67, 68].

semiconductor surface can be severely detrimental, all substrates were firstly dipped into HCl solutions (HCl : H_2O = 1 : 2). This high HCl concentration was ultimately proven to modify the InP surface (cf Chapter 2), which was unfortunately not already known during the manufacture of these samples. The subsequent metal deposition being conducted in different equipment, an air break is unavoidable after the wet surface preparation. Therefore, the wafers are exposed to a direct Ar^+ plasma etching in the deposition tool prior to the metal deposition process. As a reminder, the first two selected metallizations are the Ti and the Ni. Indeed, these two metals are very common in a front-end silicon microelectronics environment and, when used in classical contacts, both of them present very low specific contact resistivities (see Table 1.2 and Table 1.3). The 20 nm thick Ni or Ti films were deposited by DC Ar sputtering respectively at room temperature and 100 °C. All films were capped by a 7 nm thick TiN film deposited at 100 °C to protect them from any atmospheric contamination and/or oxidation. Some samples were kept as deposited while some other underwent annealing treatments in order to form intermetallic compounds at the interface between the metal and the III-V semiconductor. The majority of the samples were subjected to rapid thermal annealing (RTA/RTP) under N_2 ambient for 60 seconds at temperatures ranging from 250 °C to 550 °C. For some others, and more particularly for the Ni/InP system, isochronal long time annealing treatments consisting in a ramp up either from 50 °C to 250 °C or from 50 °C to 340 °C (1.5 °C / min) were also carried out under vacuum at 10^{-5} mbar.

3.2.2 Characterization techniques

In order to fully characterize the as deposited and the reacted films, several techniques were always coupled. The classical X-Ray Reflectometry (XRR) was mainly used to determine the thicknesses of the stacks while X-Ray diffraction (XRD) enabled the ascertainment of their composition. These characterizations were often coupled with Atomic Force Microscopy (AFM), Scanning Electronic Microscopy (SEM) and Transmission Electronic Microscopy (TEM) to check the morphology of the layers and the potential presence of amorphous compounds. In the case of non-homogeneous morphologies, localized Energy-dispersive X-ray spectroscopy (EDS) enabled the determination of the systems' compositions. Finally, thanks to High Resolution TEM (HRTEM) and Fast Fourier Transform (FFT) of the corresponding images, the crystallographic structure of the compounds could be determined. On top of these well-known characterizations, some less common technics described below were used.

X-Ray diffraction (XRD) - Detexturation

The X-ray diffraction is a non-destructive type of characterization based on the interaction of X-rays with matter. It allows the determination of the crystallographic structure of phases and relies on the Bragg's law [39]:

$$n.\lambda = 2.d_{hkl}.\sin(\theta) \qquad \textbf{Equation 3.9}$$

λ is the wavelength of the incident beam wavelength, θ is the incident angle, d_{hkl}. is the inter-reticular distance, *i.e.* the distance between two planes that belong to the same $\{hkl\}$ family, and n is an integer.

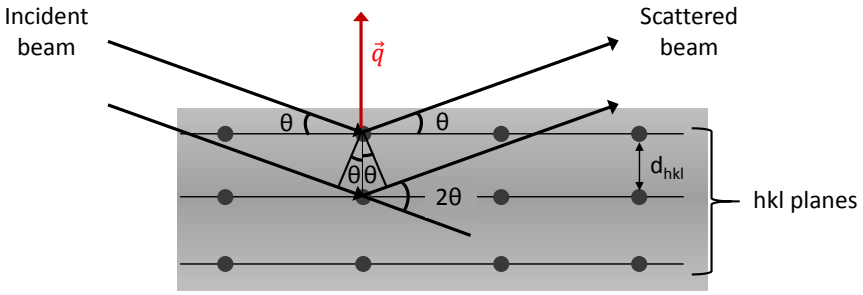


Figure 3.5: Schematic representation of diffraction of an incident X-Ray beam on atomic planes.

This equation reflects the fact that a given set of λ, θ parameters, only one family of hkl planes, *i.e.*, one crystallographic orientation gives rise to constructive interferences and therefore to a diffracted beam. When this condition is fulfilled, a peak intensity is collected by the detector. Therefore, the scanning of a large range of incident angles gives access to the crystallographic orientations represented in the compounds along with the corresponding inter-reticular distance.

However, this kind of XRD setup called Bragg-Brentano (θ/2θ) only gives access to the planes that are parallel to the surface. In this work, we deal with thin films that are often strongly textured and therefore require the use of another configuration, namely the XRD detexturation. This kind of XRD consists in acquiring θ/2θ diffractograms at several χ angles thus giving access to crystallographic orientations that are not necessarily parallel to the surface (see Figure 3.6). The sum of these diffractograms finally represents an extensive overview of the compounds crystallographic characteristics. Note that the all detexturated patterns were acquired with a 2° offset on the 2θ angle to minimize the contribution of the substrate. These final diffractograms were always firstly fitted using the software Highscore in order to determine the precise position of the peaks and the potential corresponding candidates. A manual fine tuning was then carried out to identify consistently and precisely the actual diffracting phases and orientations.

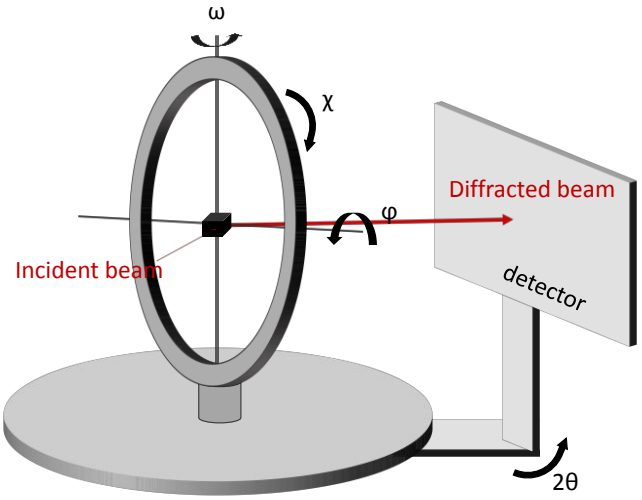


Figure 3.6: Schematic representation of an XRD setup.

The reader can refer to several books to find further precisions concerning this characterization technique [40-43].

Auger Electron Spectroscopy (AES) combined with Ar sputtering

The Auger Electron Spectroscopy (AES) is generally used to determine the surface composition of samples (around 5 nm are probed in depth). To do so, primary high-energy electrons are sent on the sample and excite the various atoms. The latter can subsequently relax thanks to the emission of Auger electrons. The kinetic energies of these emitted electrons are characteristic of the elements present in the surface of the sample. When combined with Ar^+ sputtering to abrade the sample's surface, such a technique gives access to the in-depth composition of the samples. In the experiments presented in this chapter, the AES analysis used 5 keV primary electron energy, 20 nA beam current with a diameter of 40 μm. For the depth profiling Ar^+ plasma of 1 keV energy was applied with a grazing angle of incidence with respect to the surface's normal of 80^o. All specimens were rotated during sputtering and the Ar pressure was 2.5×10^{-7} torr. After acquiring raw intensities corresponding to each investigated element, the corresponding concentrations are calculated. Various input parameters are necessary to do so, and among them the sputtering yields of the elements is crucial. The latter strongly varies with the angle of incidence in this range and corrections must therefore be applied thanks to standards. For example, in the case of samples integrated on InP wafers, the substrate is an ideal standard since it provides the Auger signals recorded using the very same parameters. To have this standard the profile should run as long as it reaches the substrate and the intensities reach stationary values. It is evident that evaluation of the substrate should result in 50 at% concentration of In and 50 at% concentration of P. Generally speaking the correction is lower than 10-15%; if it happens to be larger, the cause should be identified.

Atom probe tomography (APT)

The atom probe tomography is a characterization technique giving access to the atomic composition of samples. To perform such a characterization, the samples are shaped into a sharp tip thanks to a Focused Ion Beam (FIB) etching. The tip is cooled down and biased at high voltage (3-15 kV) which induces a very high electrostatic field (tens V/nm) at the tip surface, just below the critical point of atom evaporation. Thanks to additional laser pulses, atoms are evaporated from the surface and 36 to 50 % of them are gathered by a 2D detector. The measurement of each atoms' time of flight (TOF) gives access to the mass over charge (m/q) ratio and therefore to the nature of the atoms. The additional analysis of their impact position and arrival order on the detector allows a reconstruction of the surface atom by atom. Repeating this sequence, the whole tip is progressively evaporated and reconstructed.

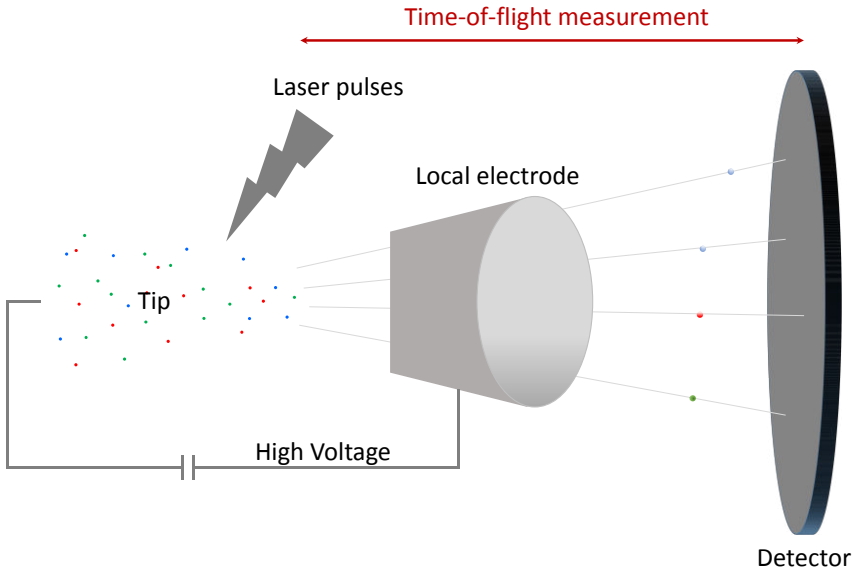


Figure 3.7: Schematic representation of the Atomic Probe Tomography (APT) setup.

Thanks to the combination of all these characterizations techniques, extensive metallurgical studies were performed. In the following sections, we will present the state of the art along with the metallurgical studies conducted on Ni/InP, Ni/InGaAs and Ti/InP systems. The reader interested in results concerning the Ti/InGaAs system can refer to Appendix A3.

3.3 State of the art about Ni-based metallizations on InP

Few studies have been reported on the formation of Ni-based intermetallic compounds on InP surfaces over the years. However, they mainly emanate from various groups, therefore offering very

different perspectives. As a result, the phase sequences related in the literature present discrepancies that will be detailed in the following section and summarized in Table 3.2 [10, 15-21].

Fatemi *et al* and Weizer *et al* report the formation of binary Ni-P phases during annealing processes lasting from 1 to 40 minutes at 400 °C [16, 19]. More precisely, after annealing treatments of a few minutes, a stack combining In, Ni_2P and Ni_3P, the latter being in contact with the InP substrate was evidenced by Energy Dispersive Spectroscopy (EDS/EDX) and AES. When this duration is extended to 40 min, they report a total consumption of the Ni_3P phase and therefore a stack composed of $In/Ni_2P/InP$. It is worth noticing at this point that the authors made a non-negligible assumption when determining the composition of the phases thanks to the AES profile. Indeed, they assumed that the totality of the In signal and the corresponding proportion of P coming from the region close to the interface actually emanated from the InP substrate.

Appelbaum *et al* report the formation of a uniform and amorphous Ni-In-P layer during the Ni deposition [20]. This amorphous layer is stable during annealing treatments at temperatures lower than 250 °C. For temperatures exceeding 250 °C, they report the non-uniform formation of a layered structure composed of binary compounds $Ni/Ni\text{-}In/Ni_xP/InP$ without specifying the exact composition of both binary phases. However, their findings differ from those of Fatemi *et al* and Weizer *et a*l as they report the stabilisation of the Ni_3P phase (24 at% P and 74 at% Ni) at temperatures higher than 400 °C. Fatemi *et al* affirm in their paper that this difference is only an apparent one [16]. Indeed, by applying their AES treatment method to the AES profile of Appelbaum *et al*, they find that the layer in contact with InP after the 400 °C annealing process is actually Ni_2P (35 %at P). This kind of intermetallic compound actually provided low contact resistivities on both n-InP and p-InGaAs and was therefore further studied [44].

Other studies from Ivey *et al* and Yamagu *et al* describe the formation of both binary and ternary phases [18, 21]. They first evidence the presence of an amorphous compound after Ni deposition, Ni_3InP, which they assume is the same as the one observed by Appelbaum *et al*. They report a laterally non-uniform crystallization from 250 °C to 300 °C leading to a sample composed of different regions where the amorphous Ni_3InP compound and the crystalline Ni_2InP coexist along with the binary Ni_2P phase. Some In is also present and oxidized at the surface leading to the presence of In_2O_3. After a 500 °C annealing treatment, they report the decomposition of the Ni_2InP phase into Ni_2P and In along with the oxidation of the latter compound. Yamagu *et al* also observed the amorphous compound for temperatures lower than 300 °C with a slightly different composition, *i.e.* $Ni_{2.7}InP$ [18]. Similarly to the previous study, this compound is decomposed and a mixture of Ni_2InP, Ni_2P and In is favored above 300 °C. The metallic In rapidly diffuses in the unreacted Ni layer and

segregates in this film and at the surface. However, in this paper the three phases are found to coexist even after a 2 minutes-long annealing treatment at 500 °C.

Contrariwise, Sands *et al* and Persson *et al* do not report the formation of binary compounds. They observe the formation of a uniform Ni_xInP (x = 2.7 and 3) phase for temperatures as low as 200 °C and 250 °C respectively [45]. This amorphous phase is shown to start crystallizing at higher temperatures, *i.e.* from 300 °C to become a hexagonal Ni_xInP phase ($3 \geq x \geq 2$). This compound finally evolves towards a fully crystallized Ni_2InP phase with a monoclinic structure after a 60-minutes thermal treatment at 360 °C. The authors precise that this phase presents a strong crystallographic texture ($[001]||[100]_{InP}$). When capped with a SiO_2 layer to prevent any P sublimation, and / or under vacuum, this compound is found to be stable up to 500 °C. Again, these authors compare their findings with the work of Appelbaum *et al* [20]. They justify the observed discrepancies by the difference in annealing ambient between the two studies. They conclude that the formation of binary compounds such as Ni_2P and Ni_2In is favored in uncapped Ni/InP systems exposed to He ambient while ternary compounds appear in capped samples. Ultimately, they come to the conclusion that the Ni-InP reactions are extremely sensitive to the annealing ambient.

In order to investigate these differences, Mohney *et al* studied bulk and thick diffusion couples (300 nm and 500 nm thick), also modifying process parameters such as the InP surface preparation and the annealing ambient [10]. Overall, they report the formation of a uniform and amorphous $Ni_x(InP)$ ($2 < x < 3$) layer in the early stages of the reaction, at temperatures as low as 250 °C consistently with the findings of Sands *et al,* Persson *et al*, Yamagu *et al* and Ivey *et al* [15, 17, 18, 21]. After thermal treatments at higher temperatures however, *i.e.* from 300 °C to 450 °C, a phase demixing associated to the formation of Ni_2P and NiIn is observed. In this range of temperatures, the Ni being partially consumed, the stack is therefore composed of $Ni/NiIn/Ni_2P/InP$. More severe annealing treatments lead to the total consumption of Ni and to the formation the monoclinic $Ni_2(InP)$ phase already observed for example by Sands *et al* and Ivey *et al* [17, 21]. Two annealing ambient, *i.e.* purified Ar gas or a mixture of Ar and H_2 (Ar-10 % H_2), were tested from 300 °C to 450 °C and did not induce any variation in the observed Ni/InP reactions. Changing the wet treatment from [H_2SO_4 (96 %) : H_2O_2 (3O %): DI H_20 = 5 : 1 : 1] to [HF (49 %):DI H_20 = 1 : 10] did not lead to any modification either. Bulk diffusion couples were finally annealed from 470 to 600 °C for durations of a few hours to several months. All of them presented the $Ni/NiIn/Ni_2P/InP$ layer sequence with no evidence of ternary phase formation. The authors explain that the formation of these binary phases is therefore an intermediate stage of the overall reaction and that the ternary phase only appears when all the Ni is consumed consistently with the ternary phase diagram presented in Figure 3.8.

They precise that the ternary Ni_2InP compound should be stable on the InP substrate up to its melting temperature, *i.e.* 526 °C [46].

In the light of the previously reported results, these conclusions seem questionable. Indeed, some authors do not observe the formation of ternary phases even when the Ni is entirely consumed, but only evidenced the presence of binary compounds [16, 19-21]. Some others do not observe a sequential appearance of the binary and ternary phases but highlight their coexistence at high temperatures [18]. It thus appears that the Ni/InP system is very complex, and might be influenced by any changes such as the Ni thickness, the thermal budget and the presence of a capping layer for example. In the following section we will present the results obtained on the Ni/InP system in our clean room and a particular focus will be made on the identification of the driving forces involved in formation of the various observed phases.

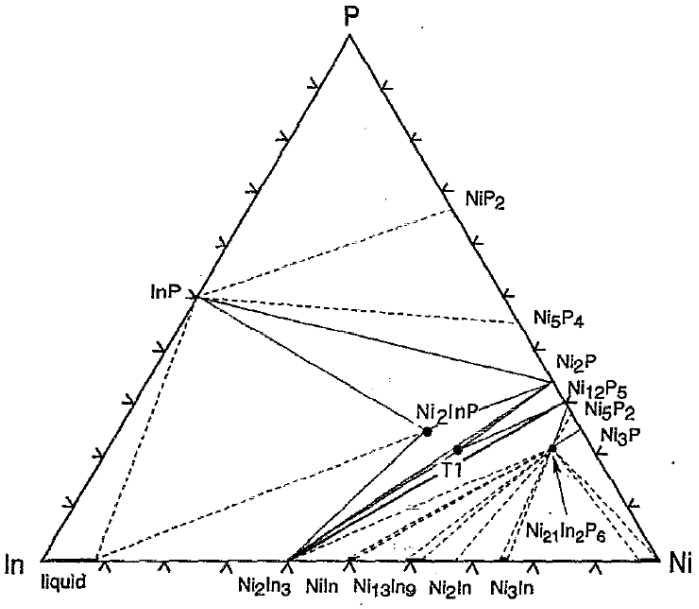


Figure 3.8: Ni-In-P ternary phase diagram at 470 °C extracted from [46]. The Ni-rich comer (dashed tie-lines) is based on a limited number of samples at 470 ° and extensive investigation at 600°C. The tie-lines to the In-rich liquid are dashed because the exact composition to which they should extend was not determined. The tie-lines to Ni_5P_4, and NiP_2 are inferred from the phase rule.

Table 3.2: Non exhaustive recapitulative table of the phase sequences observed in the literature - Ni/InP system (When encountered, N/A stands for Not Available)

Ni Thickness	Surface preparation	Deposition technique	Annealing ambient	Annealing temperature and duration	Observed compounds	Reference
200 nm	N/A	E-beam evaporation	Forming gas	400 °C – 1 min	In/Ni_2P/Ni_3P/InP	[16]
				400 °C – 40 min	In/Ni_2P/InP	
200 nm	N/A	N/A	N/A	400 °C – 4 min	In(P)/Ni_2P/Ni_3P/InP	[19]
				400 °C – 30 min	In(P)/Ni_2P/InP	
100 nm	Hot chloroform, acetone, methanol for 10 min + HF : H_2O = 1 : 10 for 60 s	E-beam evaporation	He	250 °C – 30 min	Uniform Ni-In-P/InP	[20]
				250 °C – 90 min	Ni/Ni-In/Ni_2P/InP	
				300 °C – 10 to 60 min		
				T > 400 °C	In/Ni_3P/InP	
50 nm	Polished with 5 % Br in CH_3OH solution + Rinsed in methanol+ HCl : H_2O = 1 : 1 Etched in 1 % Br in CH_3OH solution	E-beam evaporation	Vacuum of at least 10^{-4} torr	250 °C – 30 min	Amorphous Ni_xInP/InP (x ≈ 3)	[21]
				250 °C – 400 °C	In_2O_3/Ni_2InP/InP	
					In_2O_3/Ni_2InP + Ni_2P/InP	
				500 °C	In_2O_3/In + Ni_2P/InP	

Ni Thickness	Surface preparation	Deposition technique	Annealing ambient	Annealing temperature and duration	Observed compounds	Reference
300 to 500 nm	Acetone + warm methanol; rinsed in DI H_2O Etched for 60 s in [5 : 1 : 1 = H_2SO_4 (96 %) : H_2O_2 (30 %) : DI H_2O]	DC magnetron sputtering	Ar – 10 % H_2 Or Purified Ar	250 °C – 5 min	Amorphous Ni_xInP	[10]
				300 °C – 30 s	Ni/Ni-In/Ni-P/InP	
				450 °C – 30s		
				450 °C – 5 min	Ni_2InP/InP	
50 nm	N/A	E-beam evaporation	Vacuum at 1.3 x 10^{-5} Pa	250 °C – 30 min	Amorphous Ni_3InP/InP	[15]
				350 °C – 30 min	Monoclinic Ni_2InP/InP	
				500 °C – 30 min		
40 nm	H_2SO_4:H_2O_2:H_2O (5:1:1) for 2 min	E-beam evaporation	Forming gas (5 % H_2, 95 % N_2)	200°C – 60 min	Amorphous $Ni_{2.7}InP$/InP	[17]
				200°C – 15 min + 250°C – 15 min		
				200°C – 15 min + 250°C – 15 min + 300°C – 150 min	Hexagonal Ni_xInP/InP (3≥x≥2)	
				360 °C – 60s	Ni_2InP/InP	
				500 °C – 15 min		

Ni Thickness	Surface preparation	Deposition technique	Annealing ambient	Annealing temperature and duration	Observed compounds	Reference
10 nm	Ar^+ etching and H_2SO_4:H_2O:H_2O_2 = 3:1:1	E-beam evaporation	Forming gas 5 % H_2, 95 % N_2	250 °C – 2 min	$Ni_{2.7}InP$ + Ni	[18]
				300 °C – 2 min	$Ni_{2.7}InP$ + Ni_2InP + (Ni_2P)	
				400 °C – 2 min	Ni_2InP + Ni_2P + In + ($Ni_{2.7}InP$)	
				450 °C – 2 min	Ni_2InP + Ni_2P + In	
				500 °C – 2 min		

3.4 Metallurgical study of Ni-based metallizations on InP

3.4.1 Analysis of the as deposited samples

Cross sectional transmission electron microscope (TEM) samples were prepared from the as deposited Ni/InP sample by focused Ga^+-ion beam (FIB) and Ar^+-ion milling. Figure 3.9 shows the corresponding bright field TEM images on which the Ni film appears rough. This roughness was confirmed by an additional AFM characterisation where the measured height difference between the hills and valleys ranges from 15 to 20 nm (Figure 3.10). The film is polycrystalline and exhibits 50 nm wide Ni grains. The latter do not show any specific texture, but are randomly oriented as confirmed by the corresponding XRD pattern indexation presented in Figure 3.11. Note that the TiN is not observed on this θ/2θ diffractogram because it is highly textured. While some of the Ni grains are not perfectly touching each other, the TiN cap layer is primarily continuous and follows the surface topography, therefore preventing the lower layers from any contamination during samples' transfers and anneals. Additionally, an approximately 6 nm thick amorphous layer (noted α-Ni-In-P) was identified at the interface between the Ni film and the InP substrate. This observation is consistent with the findings of Ivey *et al* who also identified the presence of an amorphous compound after Ni deposition identified as Ni_3InP [21].

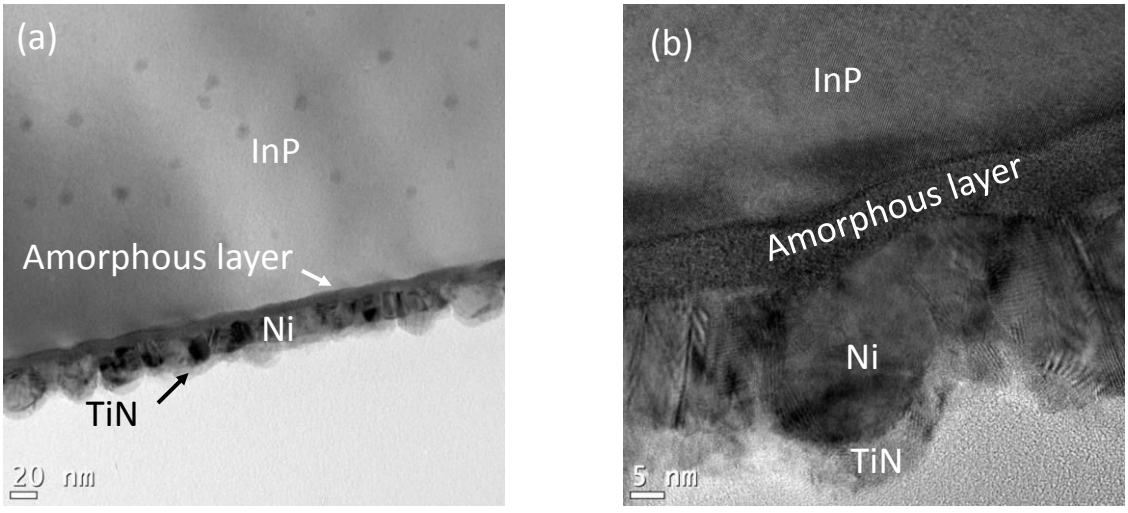


Figure 3.9: Bright field TEM image of an as deposited TiN (7 nm)/Ni (20 nm)/InP sample. The dark spots present in the InP substrate are artifacts, created during ion milling and must therefore be disregarded.

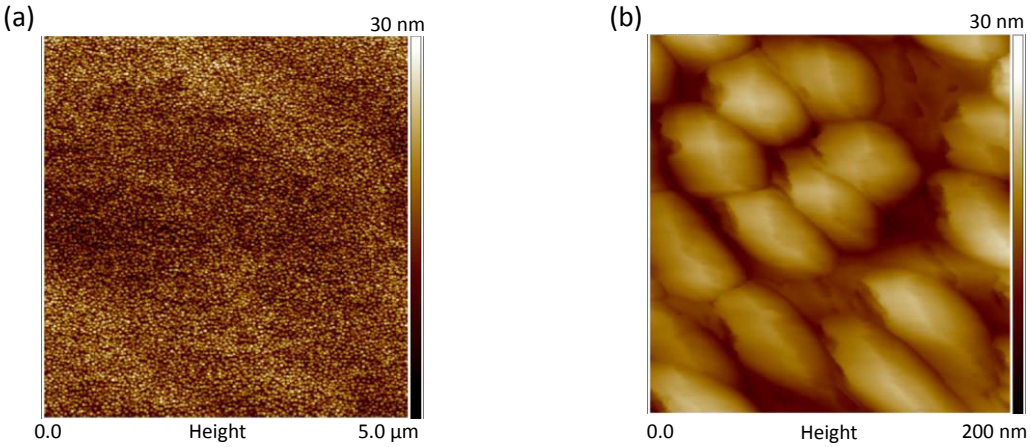


Figure 3.10: AFM images in tapping mode of the as deposited TiN(7 nm)/Ni(20 nm)/InP surface (a) 5 µm x 5 µm image area and (b) 200 nm x 200 nm scan.

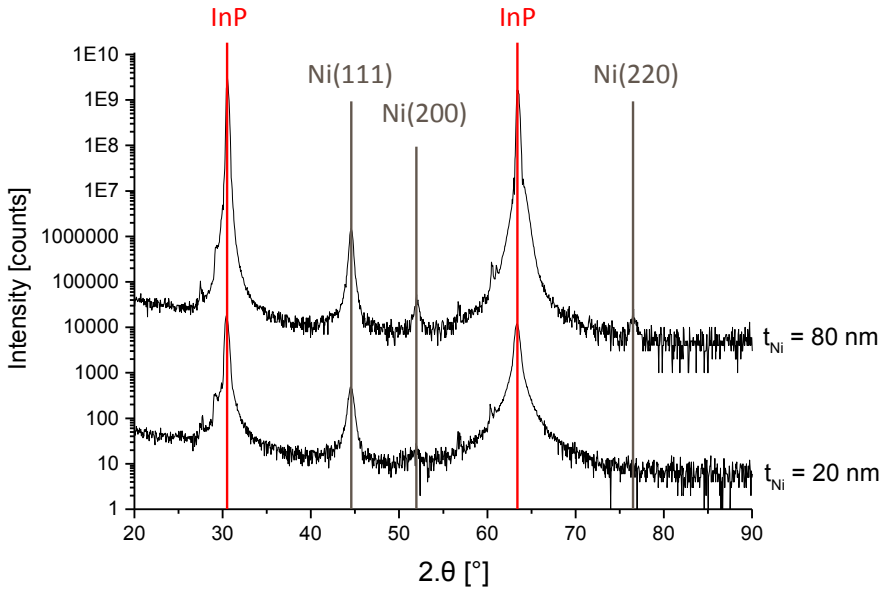


Figure 3.11: θ/2θ X-Ray diffraction pattern of the as deposited TiN (7 nm)/Ni (20 nm)/InP sample. A TiN (7 nm)/Ni (80 nm)/InP sample was also measured in order to maximize the intensity of the diffracting crystallographic orientations.

An additional AES characterization coupled with an Ar sputtering was conducted on this sample in order to determine its in depth composition (Figure 3.12). The corresponding profile is presented as a function of the sputtering time and not as a function of the depth because of the important film's roughness. Nonetheless and although it is slightly smeared by the surface roughness, this profile highlights a change of composition within this reaction product as the In/P ratio is not constant throughout the depth (Figure 3.12 (b)). The top of the layer appears to be Indium-rich whereas its bottom is Phosphorus-rich. In order to further understand this system, the next section will be

dedicated to the study of this amorphous layer and to the identification of the process causing its appearance.

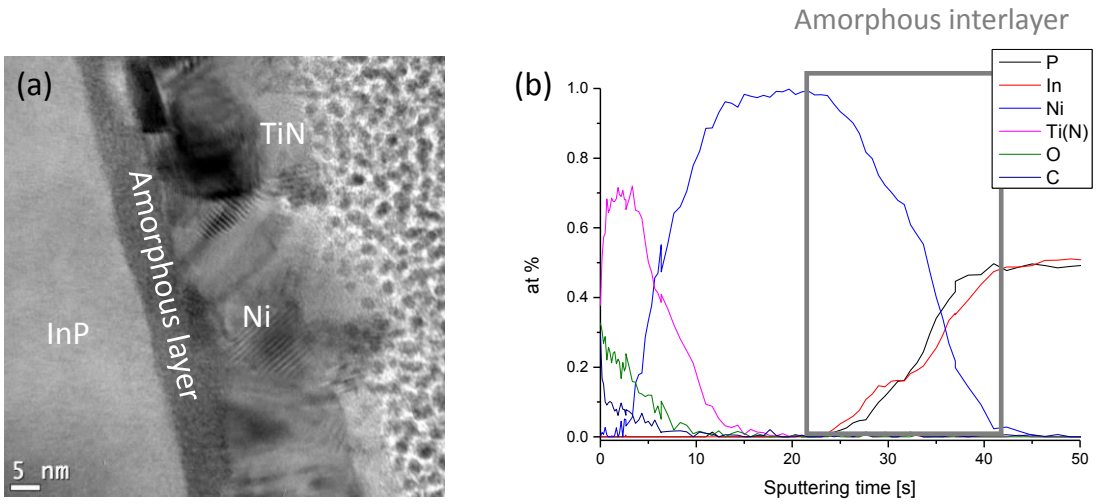


Figure 3.12: (a) TEM and (b) AES characterization of the as deposited TiN (7 nm)/Ni (20 nm)/InP sample. The grey box highlights the amorphous reaction product which is P-rich at its bottom and In-rich at its top.

3.4.2 Study of the amorphous layer on InP surfaces

In order to determine if the deposition processes were responsible for the appearance of this amorphous layer, various parameters were modified as detailed in Table 3.3.

Table 3.3: Recapitulative table of the modified parameters during the deposition of Ni and TiN (when encountered, RT stands for Room Temperature)

	Modified parameter	**Nature of the modification**
A	Ni thickness, *i.e.* duration of the Ni deposition	Divided by a factor 4 (changed from 20 nm to 5 nm)
B	Deposition rate of Ni	Multiplied by 3 (changed from 1.3 $nm.s^{-1}$ to 4 $nm.s^{-1}$)
C	Substrate temperature during the Ni deposition	Changed from RT to 150 °C
D	TiN capping layer deposited at 100 °C	Suppressed

The corresponding TEM images and AES profiles are presented in Figure 3.13. In spite of these modifications, the amorphous product along with the compositional gradient are still observed on all the samples. No amorphous layer's thickness can be extracted from the AES profiles because of the important roughness that once again smears the transitions. However, the available TEM cross

sections (samples C and D) feature amorphous layers of about 6 nm, just like it was initially observed before any process modification in Figure 3.12. Therefore, it appears that modifying the deposition temperature, rate and duration does not impact the amorphous layer.

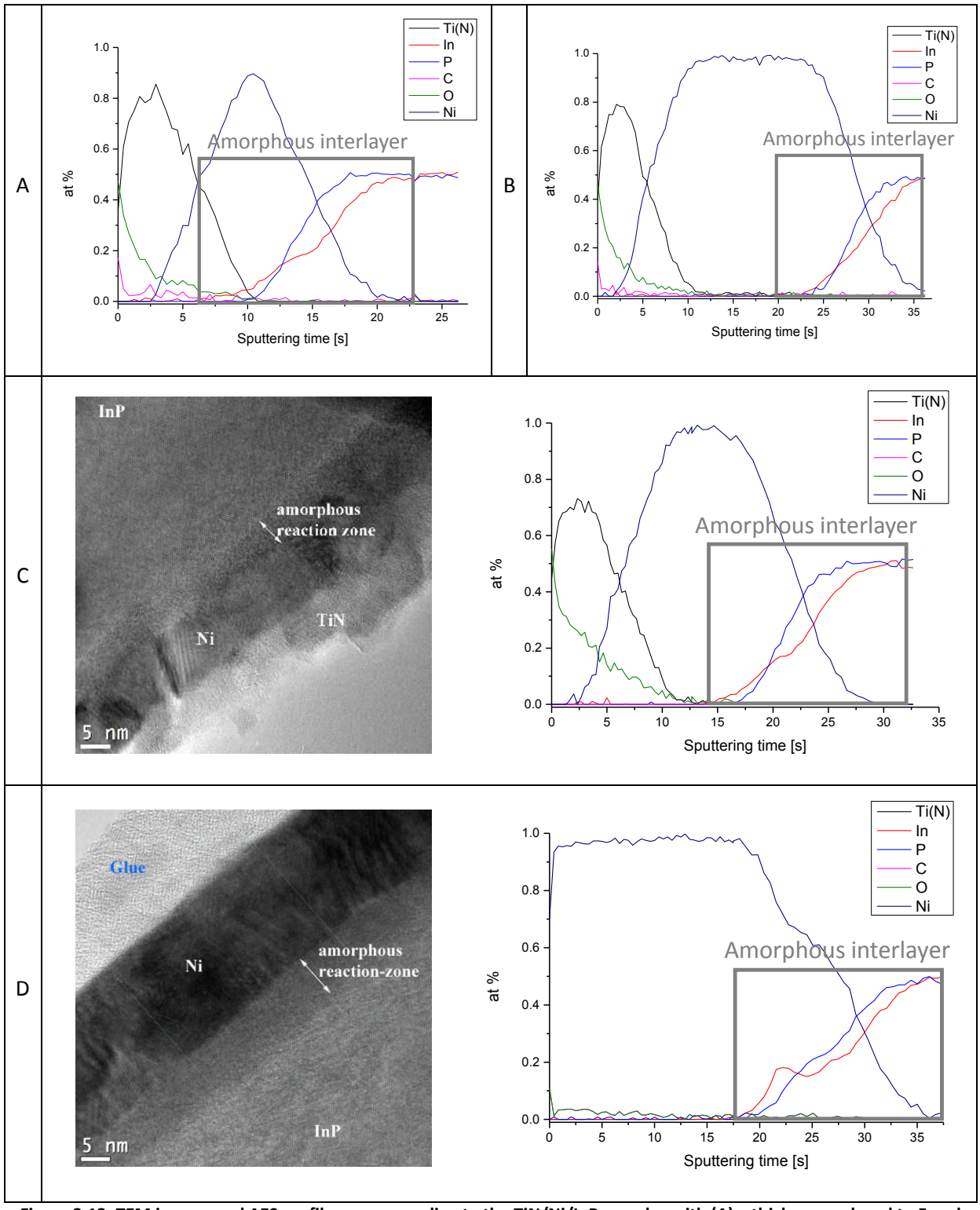


Figure 3.13: TEM images and AES profiles corresponding to the TiN/Ni/InP samples with (A) a thickness reduced to 5 and 10 nm, (B) a deposition temperature of 150 °C and (C) no TiN encapsulation.

However, as already mentioned in section 2.6.1, it has been reported in the literature that the Ar^+ plasma pre-clean modifies the substrate surface by changing the In-P bonds. According to these studies; the latter are firstly stretched and then broken, which ultimately results in P depletion of the InP surface [47-50]. Therefore, additional splits were made to investigate the effect of the Ar pre-clean on the InP surface as detailed in Table 3.4. In order to avoid Ni and InP intermixing in the amorphous layer, no Ni layer was deposited. However, a 7 nm-thick TiN layer was deposited on the samples after the dry surface preparation to prevent any parasitic oxidation and contamination of the surface.

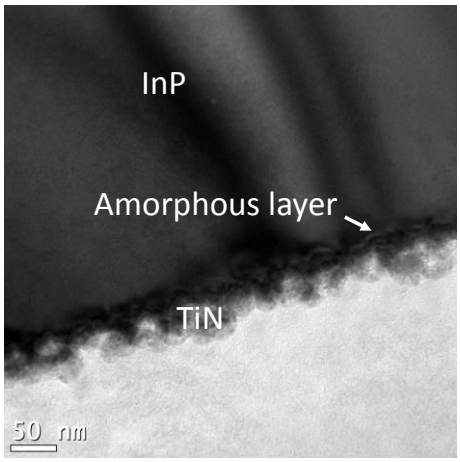
Table 3.4: Recapitulative table of the modified parameters in the plasma pre clean

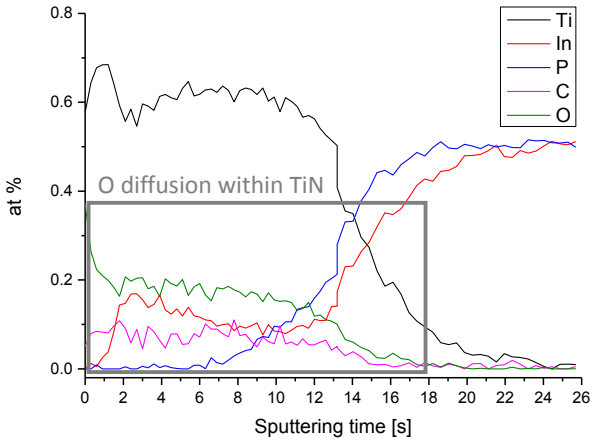
	Wet surface preparation	**Dry surface preparation**
D	HCl : H_2O = 1 : 2	Ar^+ in situ plasma treatment
E	HCl : H_2O = 1 : 2	He in situ plasma treatment
F	HCl : H_2O = 1 : 2	None

All samples were characterized by TEM and AES and the corresponding images are presented in Figure 3.14. The TEM image corresponding to the sample which was subjected to the He preclean (Figure 3.14 (E)) features an important roughness, similarly to the one observed after the Ar preclean (Figure 3.14 (D)). The TiN film is therefore discontinuous and its morphology is determined by the individual TiN grains. An amorphous layer of about 10 nm, similar to the one observed after an Ar plasma can also be identified in this case. Because of the important roughness, the corresponding AES depth profile is highly smeared and the signals emanating from the InP, the amorphous layer and the TiN top layer are not clearly distinct. Nonetheless, a clear compositional gradient can be observed on the profile. It appears therefore that this kind of plasma also leads to a phosphorus depletion of the InP surface consistently with what was previously reported in the literature [47, 49, 50]. One can notice an O signal emanating from the top region of the sample. Because of the important roughness, it would not be possible to assert if it comes from the original InP surface or from an oxidation occurring afterwards because of the TiN layer discontinuity. However, studies conducted in our group showed the efficiency of this kind of InP surface preparation and are therefore in favour of the second hypothesis [51]. When no plasma treatment is conducted, the morphology of the layers drastically changes (Figure 3.14(F)). The TiN layer observed in this case is continuous and homogeneous which results in a net AES profile. On the latter, the various layers can be clearly distinguished from one another. Particularly, the presence of an oxide on the InP surface comes as no surprise because of the absence of in situ surface preparation before the metal deposition. This native oxide, which is 2 to 3 nm thick can be seen on the corresponding TEM cross

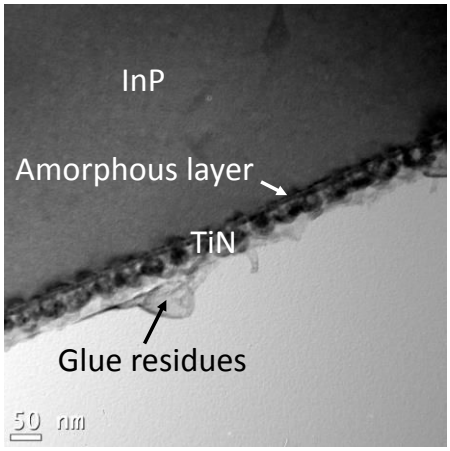
section. A slight compositional gradient is also observed within this native oxide but is much less pronounced than the one observed after an in situ preclean. It appears therefore that the wet surface preparation conducted before the in situ pre clean starts to deplete P from the InP surface. This assumption is in accordance with the findings of Cuypers *et al* who showed that, at high concentrations ([HCl] ≥ 2 M), the HCl molecule is not dissolved within the solution and anisotropically etches the InP surface [52]. This etching process results in the formation of terraces which are preferentially In-terminated. Therefore, the P depletion from InP surfaces is firstly induced by concentrated HCl solutions and strongly emphasized by in situ Ar and He-based plasma treatments. During the subsequent Ni and/or TiN deposition, which are respectively performed at room temperature and 100 °C, metal/III-V intermixing occurs and leads to the observed AES profile.

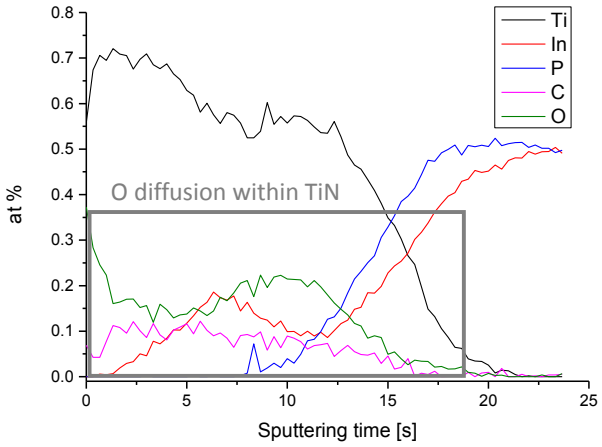
D



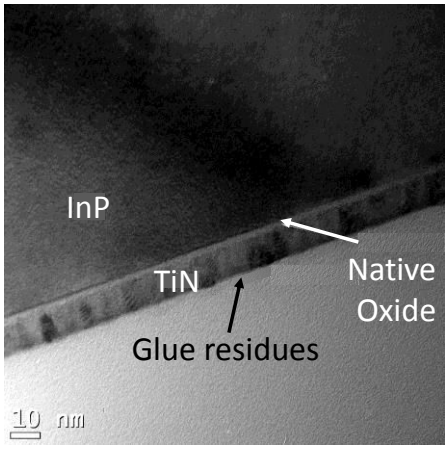


E





F



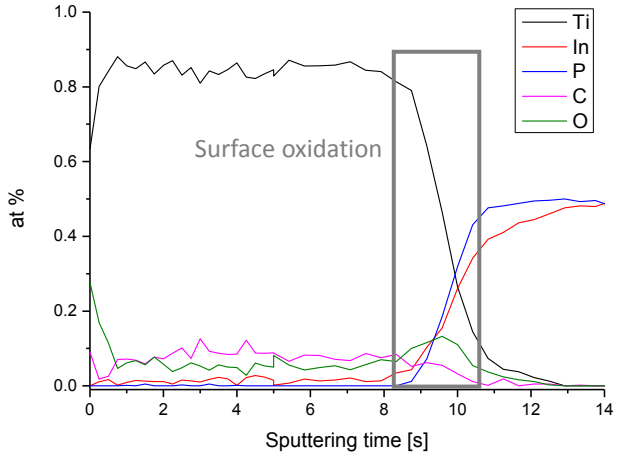


Figure 3.14: Bright field TEM images and corresponding AES profiles of TiN(7nm)/InP samples (D) with an Ar plasma preclean, (E) with an He plasma preclean and (F) without any plasma preclean.

3.4.3 Analysis of the annealed samples

In order to identify the intermetallic compounds that would be formed at the interface between the Ni film and the InP substrate, several annealing treatments were conducted. The latter firstly consisted in RTP lasting for 60 seconds at temperatures ranging from 250 °C to 550 °C. All the samples were characterized by XRD in detexturation mode, therefore giving access to the identification of the crystalline compounds (Figure 3.15). On the pattern corresponding to the mildest annealing condition tested, *i.e.* 250 °C for 60s, the presence of Ni was confirmed and no other crystalline compound was evidenced. In order to identify the thicknesses of the layers, and therefore to check the presence of any amorphous compound, an X-Ray reflectometry characterization was performed. The latter revealed a stack with a total thickness of 34 nm, most likely corresponding to the already observed stack just after the metal deposition: TiN(7 nm) / Ni(20 nm) / α-Ni-In-P (6 nm) / n-InP. This finding is consistent with the works of Appelbaum *et al*, Ivey *et al*, Mohney *et al*, Persson *et al*, Sands *et al* and Yamagu *et al* who observed the presence of the amorphous $Ni_{2-7}InP$ layer after thermal treatments conducted a 250 °C [10, 15, 17, 18, 20, 21].

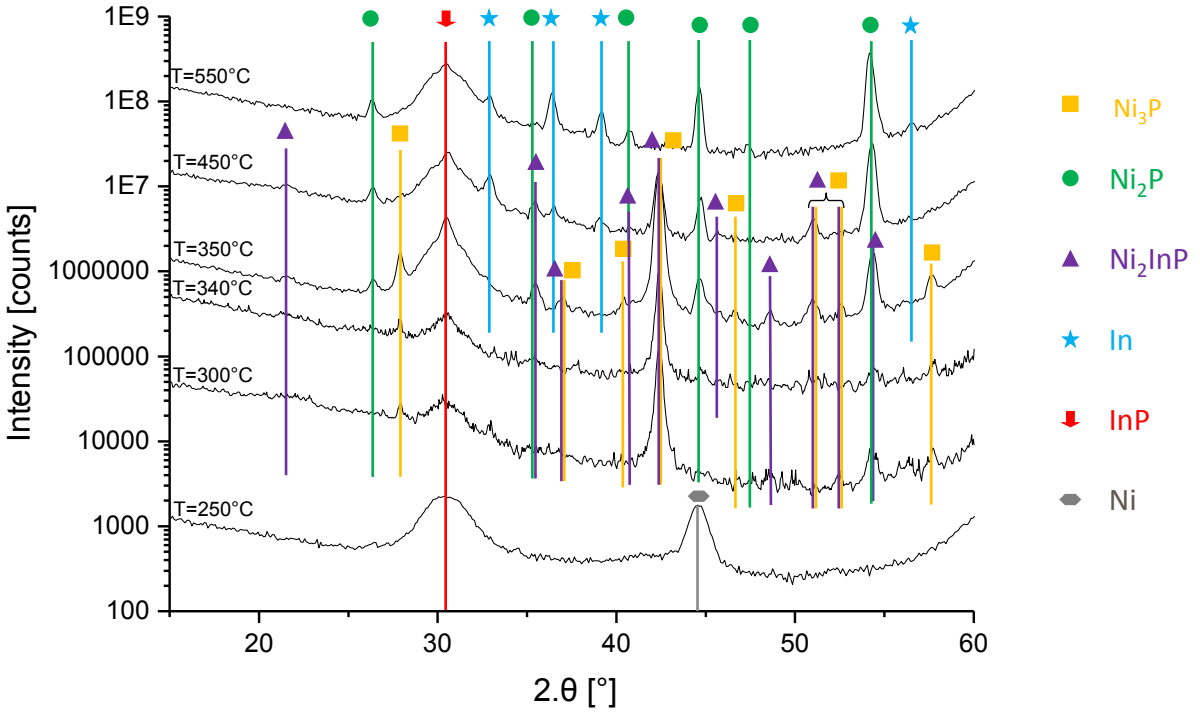


Figure 3.15: θ/2θ XRD patterns of the Ni/InP samples annealed at 250 °C, 300°C, 340°C, 350 °C, 450 °C and 550 °C for 60 seconds (RTP). A 2° offset on the incident beam was applied in order to minimize the InP substrate contribution.

The RTP conducted at 300 °C lead to major modifications of the system. Indeed, it resulted in the consumption of the Ni while binary and ternary compounds, namely the hexagonal Ni_2P, the

tetragonal Ni_3P and the monoclinic $Ni_2(InP)$, were formed (Figure 3.15). It is to note that while some peaks are unique for each phase, Ni_2P (44.7°, 47.3°), Ni_3P (27.9°, 46.6°, 57.6°), $Ni_2(InP)$ (21.6°, 45.7°, 48.6°), others may be attributed to a combination of two compounds (for example at 42.4° and 50.6°). No modification of the observed composition was brought by increasing the annealing temperature up to 340 °C. However, an augmentation of the peak intensities at 350 °C highlighted the growth of the three compounds. Meanwhile, several peaks were attributed to the tetragonal In phase (32.9°, 36.3°, 39.1°, 56.6°), revealing the presence of crystalline In at this temperature. In order to further characterize this sample a bright field TEM analysis was conducted along with a mapping of the Ni. These characterisations where conducted on two parts of the same sample glued together face to face. The corresponding cross-section presented in Figure 3.16 (a) indicates the presence of a 60 nm thick layer which is fully crystalline. As a consequence, accordingly with the literature, it appears that the amorphous layer was consumed or crystallized during the binary and ternary phases formation at 350 °C [10, 15, 17, 21]. However, the two analysed parts of the sample exhibit very different morphologies. Indeed, while one presents a uniform and continuous layer, the other presents isolated grains. The corresponding mapping shows that the Ni is only contained in either layer or the grains while the other regions are Ni-free (Figure 3.16(b)). Analysing this sample thanks to an AFM measurement gave access to the morphology of the overall surface (Figure 3.17). It appears that the surface presents an important roughness with elongated, “boat-shaped” Ni-containing agglomerates. This kind of morphology most likely has its origins in the wet surface preparation of the InP surface. Indeed, the studies that we presented in section 2.6.1, evidenced a similar InP surface morphology after being dipping in a $HCl:H_2O$ = 1:2 solution. Therefore, it is very probable for the thermal treatment to reveal the substrate surface morphology up to the metallic layers. The resulting cross sections display continuous layers when the protrusions are cut along their long-axis, and individual grains when they are cut along their short-axis.

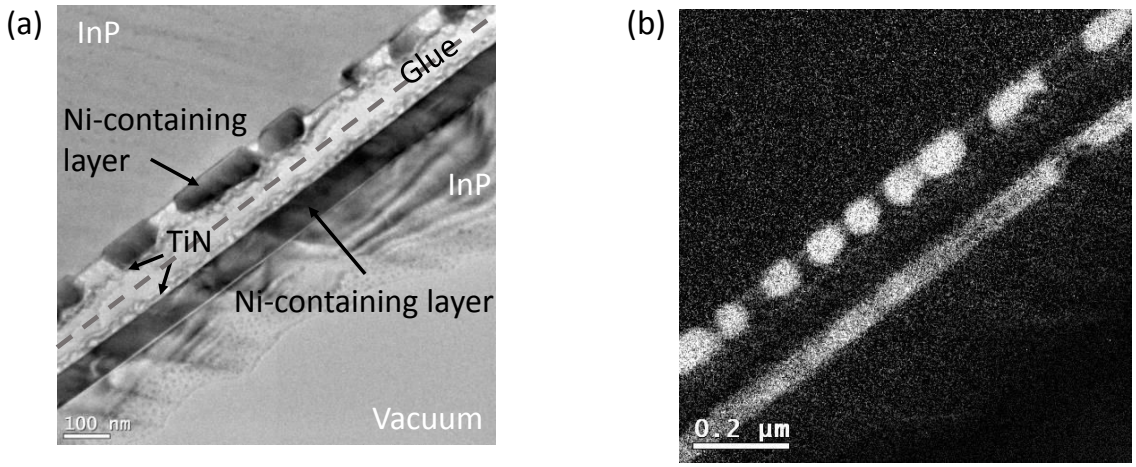


Figure 3.16: (a) Cross sectional bright field TEM image of the Ni/InP sample after a 60-second RTP at 350 °C and (b) corresponding Ni mapping.

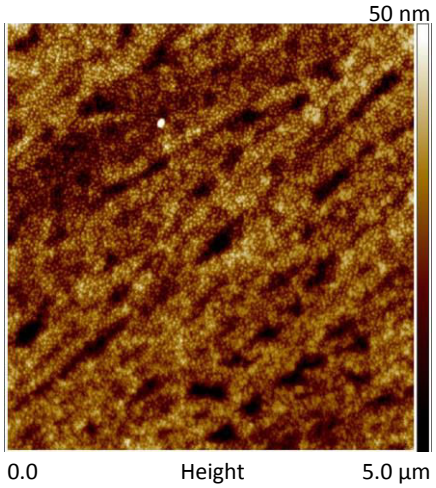


Figure 3.17: AFM measurement in tapping mode of the sample TiN(7 nm)/Ni(20 nm)/InP annealed at 350 °C for 60 seconds (image area is 5 µm x 5 µm).

When the temperature of the annealing treatment is brought up to 450 °C, the Ni_2(InP) as well as the Ni_3P phases are partially consumed while In (32.9°, 36.3°, 39.1°, 56.6°), and Ni_2P (26.4°, 44.7°, 47.3°) start to prevail. This behaviour was enhanced by the increase of the temperature as the system was composed of Ni_2P and In after the 550 °C RTP. A bright field TEM image of this sample combined with an EDS analysis confirmed this conclusion and showed that the Ni_2P is agglomerated and surrounded by the In phase at this temperature (Figure 3.18 (a) and (b)). It is important to note that the spatial resolution of the EDS analysis does not allow a perfect distinction of the In lobes which explains the presence of some In and P peaks in the corresponding spectrum. Agglomerates similar to the one presented in Figure 3.18 are distributed all over the InP surface and are generally separated from one another by a gap of 400 to 600 nm. Finally, the In which is present all around the Ni_2P agglomerate looks like it went through liquid state during this RTP.

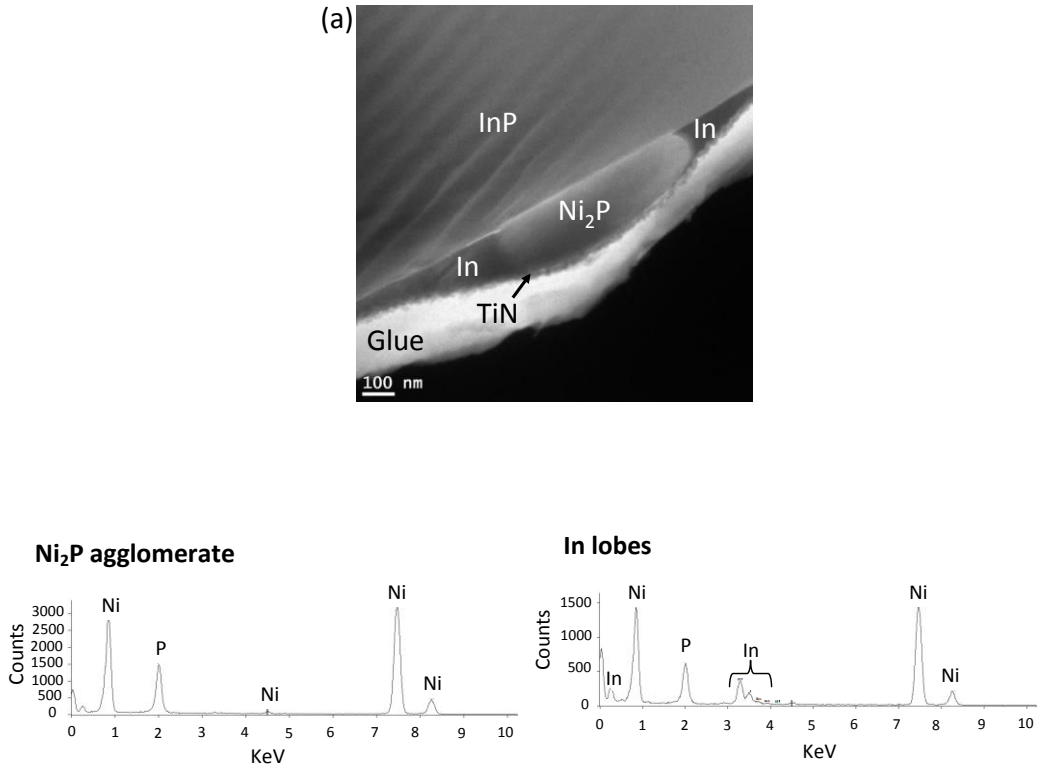


Figure 3.18: (a) Cross sectional bright field TEM image of the Ni/InP sample after a 60-second RTP at 550 °C; (b) EDS spectra of the the central Ni_2P grain and the two In lobes.

The phase sequence that was identified thanks to RTP annealing treatments is recapitulated in Figure 3.19 in bold colours. For temperatures that were not investigated, trends on the phases' evolution are displayed with a light filling.

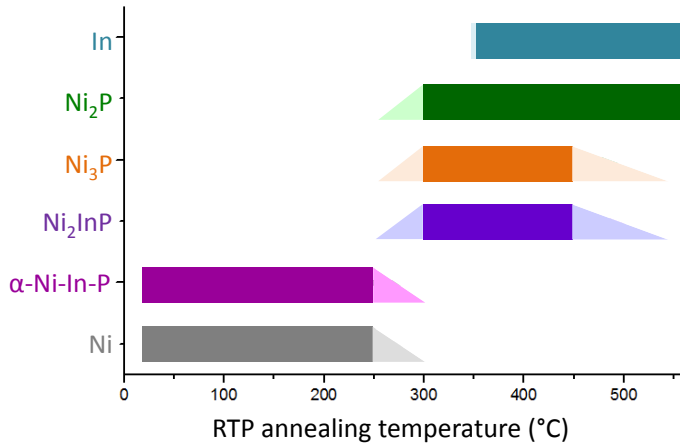


Figure 3.19: Recapitulative chart of the observed (bold filling) phases on Ni/n-InP layers as a function of the annealing temperatures (duration = 60 s). The light fillings correspond to temperatures that were not investigated and for which only trends on the phases' evolution are displayed.

3.4.4 Discussion

The formation of reliable and reproducible ohmic contacts relies on the understanding of the driving forces responsible for the formation of the observed compounds. Particularly, it is of great interest to identify if the formation of the various phases is simultaneous or sequential. In the latter case, determining the order of appearance of the phases is relevant as it opens the possibility to promote the electrically favourable compounds by adjusting the duration and the temperature of the annealing treatment. In order to determine the order of appearance of the phases and the associated mechanisms, additional longer anneals were performed. The latter consisted in a ramp up from room temperature to 340 °C with a slope of 1.5 °C per minute.

In situ XRD characterizations

First of all, classical θ/2θ XRD characterizations were performed during this annealing treatment every 1.5 °C, therefore enabling the identification of the sample's compositions at each temperature. The resulting 2D projection is presented in Figure 3.20. The latter highlights the partial consumption of the Ni phase from 170 °C along with its total consumption at 270 °. The absence additional peaks corresponding to intermetallic compounds in this range of temperatures can be attributed to an amorphous nature of these compounds, or to crystalline compounds presenting a volume too low to generate observable diffraction peaks. However, from 270 °, the pattern features peaks that can be attributed to the binary and ternary phases Ni_3P, Ni_2P and Ni_2InP. However, while some peaks allow a confident identification of the Ni_3P phase (57.7 °, 27.8 °) some other can be attributed to two different phases (42.4 °, 40.7 °). Moreover, the number of diffraction peaks is very low compared to the patterns obtained thanks to the XRD detexturation at comparable temperatures (Figure 3.15). It is therefore highly probable that the compounds present in the sample are textured and do not diffract in a classical θ/2θ XRD mode. As a consequence, the identification of the sample's composition at each temperature was not enabled by this kind of setup and XRD detexturations appeared to be a necessity. However, such measurements are very long as they often last for 10 hours and therefore could not be performed during the annealing treatment. To address this issue two samples were submitted to the same annealing treatments, either up to 250 °C or to 340 °C and were characterized thanks to ex situ XRD detexturation. The corresponding XRD patterns are presented and compared to the ones obtained after the RTP respectively in Figure 3.21 and Figure 3.22.

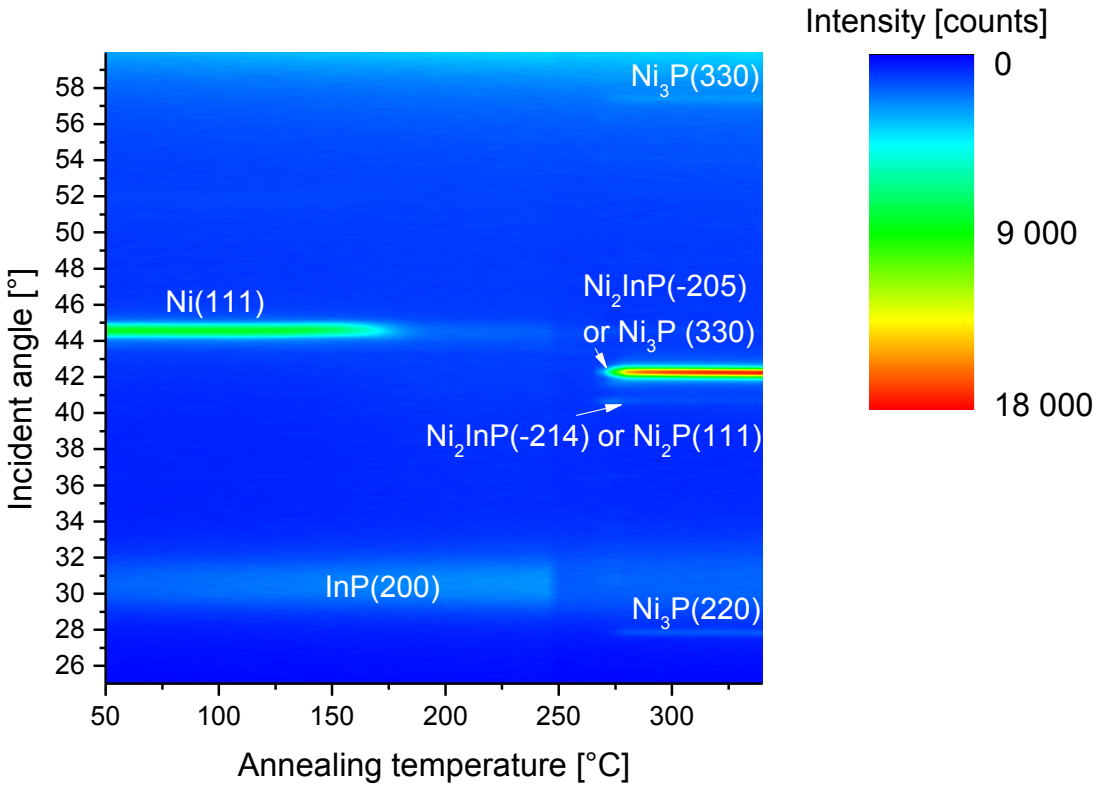


Figure 3.20: 2D projection of the θ/2θ diffractograms obtained during an isochronal annealing treatment from RT to 340 °C. Diffractograms were acquired every 1.5 °C and the total duration of the ramp up was 7 hours.

Formation of the binary and ternary phases

As shown in Figure 3.21, increasing the annealing duration at 250 °C resulted in a strong modification of the observed composition. While the Ni containing layer was still present after the 250 °C – 60 s RTP, it had disappeared after the long-time annealing process (5 hours). The latter resulted in the formation of the binary and ternary compounds, namely Ni_2P (47.3°), Ni_3P (e.g. at 27.9°, 57.6°) and $Ni_2(InP)$ (*e.g.* at 32.7°, 33.4°, 44.4°). Thus, it appears that the formation of this compounds is not limited by the supply of thermal energy and therefore by the overcoming of any nucleation energy barrier. On the contrary, it only requires a duration long enough for the reactions to occur. As detailed in section 3.1.2, this means that the kinetics are controlled by the speed at which the interfacial reactions actually occur and by the speed at which the species can reach the interface, *i.e.* by the diffusion. As it was already observed for the silicides Ni_2Si and NiSi in [33], the formation of Ni_2P, Ni_3P and Ni_2InP is therefore ruled by the linear-parabolic law.

Additionally, while the initial system was composed of Ni and an amorphous α-Ni-In-P layer, the long-time annealing process resulted in the formation of two binary Ni-P phases, Ni_2P and Ni_3P, and one ternary phase, $Ni_2(InP)$ that conserves the substrate stoichiometry. As the overall composition must

be conserved through the metallurgical reactions, the formation of these binary and ternary phases must be associated to some atomic In release. Because the corresponding diffractogram does not feature any In peak, this compound must be directly rejected in the lattice during the formation of the intermetallic compounds. At this point, two hypotheses can be made: (i) the In can be nanocrystallized with a diffracting volume too small to be detected by the XRD and (ii) the In can be dissolved and distributed in the lattice without nucleating. Further studies concerning the appearance of the In phase at 350 °C during RTP treatments will be presented in the following section and lead us to exclude the first hypothesis as the nucleation of In at 250 °C is highly improbable. Therefore, it is very likely that the In is partitioned in the lattice during the formation of the different for temperatures lower than 350 °C.

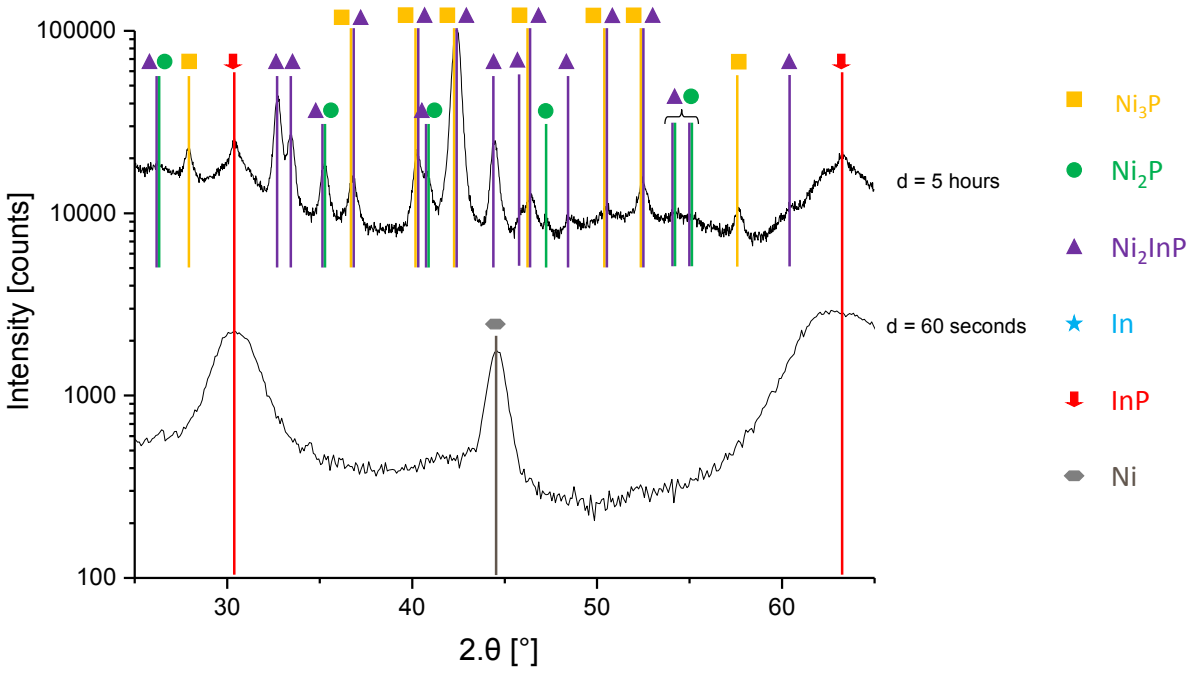


Figure 3.21: θ/2θ XRD pattern after the 60-second RTP and XRD detexturation pattern after the long-time anneal up to 250 °C (ramp up duration = 5 hours) of the Ni/InP system.

In distribution during Ni/InP reactions

However, at 350 °C the XRD pattern displayed in Figure 3.15 indicates the signs of a nucleated and crystalline In phase. To investigate the driving forces involved in this process, an additional 7 hours-long thermal treatment was conducted at 340 °C. The XRD detexturation patterns corresponding to this sample and to the ones annealed at 340 °C and 350 °C for 60 seconds are presented in Figure 3.22. As indicated by the indexation of the peaks, increasing the annealing duration from 60 seconds to 7 hours at 340 °C led to the promotion of the Ni_2(InP) phase. However, the longer annealing

duration did not have any impact on the In behaviour as the system does not show any sign of crystalline In at this temperature. On the contrary, a 10 °C rise led to the appearance of In peaks (32.9°, 36.3°, 39.1°, 56.6°) on the XRD pattern. Based on these observations two hypotheses can be made to explain the appearance of these peaks: the In might go through (i) a melting/solidification process or (ii) a precipitation process at 350 °C.

(i) As indicated in Figure 3.22, increasing the duration of the heat treatment at 340 °C favoured the growth of the Ni_2(InP) phase while the binary phases seem more or less stable. On the contrary, increasing the temperature to 350 °C led to the growth of two phases (Ni_2P and Ni_3P) at the expense of the Ni_2(InP) phase in which case a larger amount of In is released. When the quantity of In is important enough, and since the In melting temperature is exceeded (T_M = 156 °C), it might start melting. Then, during RTA quenching, the In solidification process takes place and leads to the formation of In agglomerates. Consequently, it would mean that Ni_2P and N_3P kinetics are too slow at 340 °C and limit both phases' growth as well as In release. Therefore In concentration remains too low to melt until the system reaches 350 °C. The limitation to this theory is that one would expect to see the In phase with a rounded shape (coming from the liquid phase) or at least a non-homogenous layer on the corresponding TEM cross section while none of these two features can be observed (Figure 3.16).

(ii) A second hypothesis can explain the appearance of In peaks at 350 °C. As in theory (i), In must be redistributed/partitioned in the lattice during the formation of the binary and ternary phases. At temperatures lower than 350 °C and even if the amount of released In is large enough, the thermal energy may not be important enough to enable the nucleation of In precipitates. On the contrary, for temperatures equal to or greater than 350 °C, nucleation may occur therefore leading to the formation of diffracting In precipitates. In this second hypothesis, the kinetics of In phase formation would then be limited by the nucleation in which case the In would not go through a liquid phase.

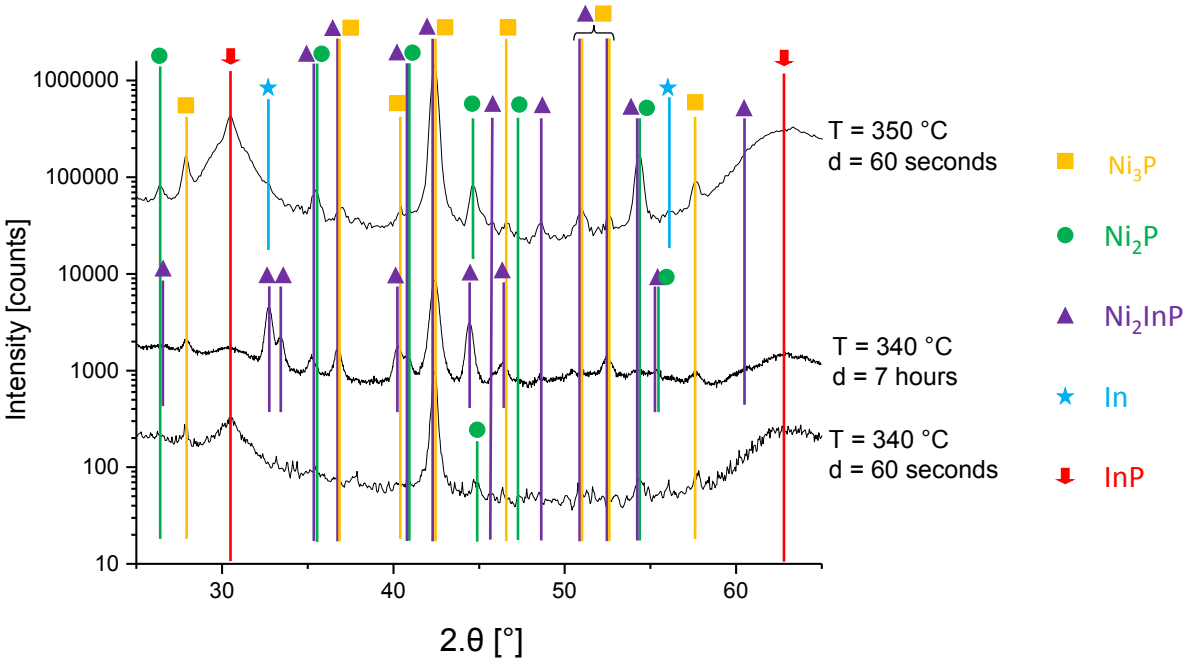


Figure 3.22: θ/2θ XRD pattern after the 60-second RTP at 340 °C and 350 °C and XRD detexturation pattern after the long-time anneal up to 340 °C (ramp up duration = 7 hours) of the Ni/InP system.

3.4.5 Summary of the results

We demonstrated that the InP substrate cleaning procedure, which includes an Ar^+ plasma in situ pre-clean prior Ni deposition results in the modification of the surface by creating a non-homogeneous α-Ni-In-P amorphous layer. After 60 s-RTP on Ni (20 nm) / InP, we showed that the phase sequence involves the coexistence of binary and ternary phases (Ni_2P, Ni_3P and $Ni_2(InP)$) which formation must be associated with some In partitioning in the early stages of the reaction. We assume that the Ar^+ plasma pre-clean could play an important role in this phase sequence as it results in P depletion of the substrate's surface. We also demonstrated that for a short annealing duration (60 seconds) the binary Ni_2P phase grows at the expense of Ni_3P and $Ni_2(InP)$ as the annealing temperature increases. This process is accompanied by In precipitation or melting / solidification for temperatures equal to or greater than 350 °C. The various characterisations highlight the fact that the making of the binary and ternary compounds is not controlled by the nucleation but by the diffusion and/or by the interfacial reaction. Finally, we evidenced the formation of In clusters from 350 °C and we discussed two different hypotheses to explain their appearance: In melting/solidification or In precipitation controlled by the nucleation. These results are summarized in Figure 3.23.

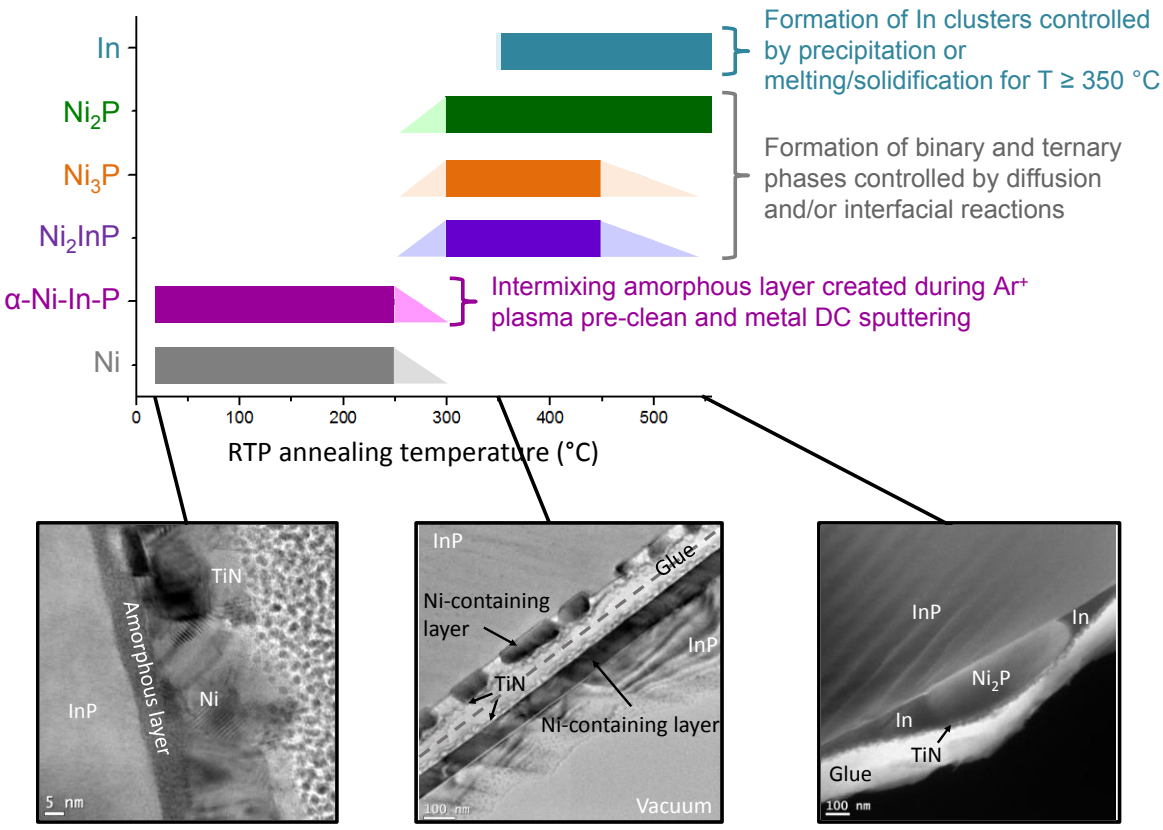


Figure 3.23: Summary of the metallurgical study conducted on the Ni/InP system. The light fillings correspond to temperatures that were not investigated and for which only trends on the phases' evolution are displayed.

3.5 State of the art about Ni-based metallizations on InGaAs

The properties of Ni-(In)GaAs contacts have been studied over the years for the purpose of forming self-aligned contacts that could be integrated on III-V MOSFETs devices [11-13, 22-29]. Most studies report the formation of quaternary coumpounds for temperatures as low as 250 °C. However, up to the 2010's, metallurgical studies were mainly focused on the Ni/GaAs system and there was a lack concerning the Ni/InGaAs system. Because understanding the material properties such as the crystal structure, the lattice parameters and the epitaxial relationship with the underlying InGaAs is imperative, extensive studies were conducted in the past few years. The latter also deal with the ratio of Ni to Ni-InGaAs thicknesses and the thickness uniformity of the reaction product that are key parameters to decrease the resulting series resistance in the devices. A summary of the phase sequences reported in the literature can be found in Table 3.5.

Zhang *et al* studied the as deposited and annealed Ni/InGaAs systems through XRD and TEM cross sections [11]. Thanks to these characterizations, they were able to identify the polycrystalline nature of the 30 nm thick Ni film deposited by sputtering. The latter appears to be stable at least up to

200 °C. However, after a thermal treatment lasting for 60 seconds at 250 °C, they observed the total consumption of the Ni and the formation of a crystalline quaternary compound. The latter was found to be uniform and 45 nm thick. Thanks to localized EDX measurements, the composition of the layer was identified as Ni:In:Ga:As = 51:12:14:23. On top of this metallurgical study conducted on blanket wafers, the authors integrated this compound on actual MOSFETs devices in other studies [22-24]. The additional steps necessary for the patterning of the devices did not seem to affect the nature of the layer which was still composed of the same intermetallic compound (Ni:In:Ga:As = 51:13:15:21). One interesting attribute lies in the fact that the authors were able to selectively remove the unreacted Ni thanks to an HCl solution [53]. This feature strongly facilitates the overall contact integration as it opens the way to a self-aligned metallization.

Shekhter *et al* and Mehari *et al* report the formation of a similar compound at 250 °C. Thanks to EDS and XRD characterizations, they were able to identify this compound as being the hexagonal $Ni_2In_{0.53}Ga_{0.47}As$ (Ni:In:Ga:As=4:1:1:2) [12, 13]. According to their findings, the initial 6 nm of Ni give rise to a 12 nm thick Ni-InGaAs layer which is in epitaxial relationship with the underlying substrate.

The most complete study probably comes from Ivana *et al* [28]. In the latter, the Ni films are deposited and subjected to annealing treatments at various temperatures (from 200 °C to 350 °C) for various durations (20 to 60 seconds). A very thin intermixed region is identified right after DC sputtering deposition at the interface between the Ni and the InGaAs. A SIMS characterization showed that the latter is thickened by an annealing treatment conducted at 200 °C for 60 seconds. However, no crystalline compound other than the Ni was identified at this temperature by XRD. Increasing the temperature up to 250 °C lead to the total consumption of Ni and to the formation of a quaternary compound for durations as low as 20 seconds. The thickness ratio between the deposited Ni and the Ni-InGaAs reaction product was found to be 1:1.7. Moreover, this product was identified by XRD, EDX and XPS as being $Ni_4InGaAs_2$ with a B8 hexagonal structure. Selected Area Diffraction (SAD) showed that this compound is highly textured and presents an epitaxial relationship with the InGaAs. It is important to note that the authors do not exclude the fact that the quaternary compound's formation might be initiated at temperature comprised between 200 °C and 250 °C. Anyhow, the authors assume that the mechanism involved in the reaction between Ni and InGaAs might be comparable to that of Ni/GaAs. This means that Ni atoms would predominantly diffuse through interstitial sites in the Ni-InGaAs phase to reach the Ni-InGaAs/InGaAs interface where the solid state reactions take place. According to them, this process probably involves breaking In (or Ga)-As bonds and forming In (or Ga)-Ni bonds and As-Ni bonds. At 300 °C, two additional diffraction peaks attributed to $Ni_4InGaAs_2$ appear on the XRD pattern. The latter suggest that the orientation of the intermetallic compound is slightly modified between the two temperatures. However, at 350 °C

the intermetallic compounds' composition probably slightly changes and a new phase which composition is not reported appears.

For the first time, Chen *et al* conducted a similar metallurgical study in fin structures in 2015, *i.e.* under scaled-down dimensions (from 30 to 500 nm) [27]. While the kinetics seem to be influenced by the dimensions of the contacts, the compound ultimately observed between 250 °C and 300 °C is still the hexagonal $Ni_4InGaAs_2$. In accordance with Mohney *et al*, the Ni is found to be the main diffusing species during the formation of the Ni-InGaAs intermetallic compound.

Even though a unique phase sequence was observed in the above mentioned studies, Zhiou *et al* report original results [29, 54]. The authors conducted extensive XRD characterizations and pole figures measurements from which they extract the phases' crystallographic structures and stoichiometries. Unlike the other authors, Zhiou et *al* did not observe the reaction of the 20 nm thick Ni film at 250 °C which requires a temperature of 300 °C to be initiated. After the latter annealing treatment, they showed that the c/a ratio corresponds to the $Ni_3In_{0.53}Ga_{0.47}As$ phase. The already observed $Ni_2In_{0.53}Ga_{0.47}As$ is only present after the annealing treatment conducted at 450 °C and is not stable at higher temperatures. Indeed, the formation of a NiAs-like phase is observed at 550 °C as the intermetallic tends to expel Ga and In atoms at high temperatures. On top of that, thanks to in situ measurements, the authors showed that although the transition from $Ni_3In_{0.53}Ga_{0.47}As$ to $Ni_2In_{0.53}Ga_{0.47}As$ is accompanied with a modification of the diffracting peaks' position (shift > 2°), the transition from $Ni_2In_{0.53}Ga_{0.47}As$ to NiAs only results in a small shift linked to the distortion of the lattice (shift < 0.3°) [54].

As a consequence, similarly to the Ni/InP system, no consensus is reached concerning the phase sequence observed in the Ni/InGaAs system. However, the authors agree on the fact that the Ni diffusion is responsible for the appearance of the observed intermetallic compounds at low temperatures. In the following we will present similar metallurgical studies conducted on blanket wafers along with the obtained results.

Table 3.5: Non exhaustive recapitulative table of the phase sequences observed in the literature - Ni/InGaAs system (When encountered, N/A stands for Not Available)

Ni Thickness	Surface preparation	Deposition technique	Annealing ambient	Annealing temperature and duration	Observed compounds	Reference
30 nm	Dilute Hydrofluoric acid	Sputtering	N_2	250 °C - 60 s	Uniform and crystalline Ni-InGaAs (Ni:In:Ga:As = 51:12:14:23) 45 nm thick	[11]
11 and 28 nm	Dilute Hydrofluoric acid	DC sputtering (P = 200 W)	N_2	As deposited	Ni/Ni-InGaAs /InGaAs	[28]
				200 °C – 60 s		
				250 °C – 20 s	Hexagonal $Ni_4InGaAs_2$/InGaAs In epitaxial relationship with InGaAs	
				300 °C – 60 s		
6 nm	H_2SO_4:H_2O=1:10 Rinse in DI	e-beam evaporation	Forming gas (10% H_2)	250 °C – 60 s	Hexagonal $Ni_4InGaAs_2$/InGaAs In epitaxial relationship with InGaAs	[12, 13]
200 nm	HF	e-beam evaporation	N/A	250 °C to 300 °C	Hexagonal $Ni_4InGaAs_2$/InGaAs	[27]

Ni Thickness	Surface preparation	Deposition technique	Annealing ambient	Annealing temperature and duration	Observed compounds	Reference
20 nm	Ar^+ plasma	RF-PVD	N_2	250 °C – 60 s	Ni/InGaAs	[29]
				300 °C – 60s	$Ni_3In_{0.53}Ga_{0.47}As$ /InGaAs	
				450 °C – 60 s	$Ni_2In_{0.53}Ga_{0.47}As$ /InGaAs	
				550 °C – 60 s	NiAs-like phase /InGaAs	

3.6 Metallurgical study of Ni-based metallizations on InGaAs

3.6.1 Analysis of the as deposited Ni/InGaAs

The as deposited Ni/InGaAs sample was firstly characterized by XRD in order to determine its composition along with the crystallographic orientation(s) of the compounds. The corresponding XRD pattern is presented in Figure 3.24.

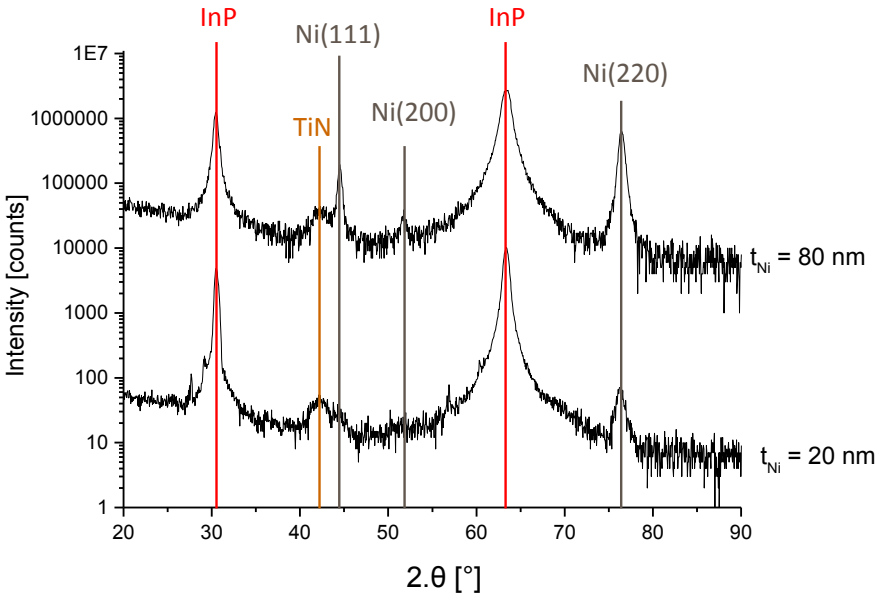


Figure 3.24: θ/2θ X-Ray diffraction pattern of the as deposited TiN (7 nm)/Ni (20 nm)/InGaAs sample. A TiN (7 nm)/Ni (80 nm)/InGaAs sample was also measured in order to maximize the intensity of the diffracting crystallographic orientations.

The as deposited Ni film appears to be polycrystalline on InGaAs just like it was on InP substrates. The XRD patterns do not indicate the formation of any other crystalline compound during the deposition of the Ni and TiN layers, respectively conducted at room temperature and 100 °C. The corresponding TEM cross section seems to confirm this hypothesis as it highlights the presence of continuous and homogeneous Ni and TiN layers separated by flat and sharp interfaces (Figure 3.25(a)). The measured thicknesses also correspond to the deposited ones as the Ni and TiN layers are respectively 20 and 7 nm tick. However, in spite of the very sharp interfaces, the corresponding AES characterization displays diffusion profiles both at the bottom and at the top of the Ni layer (Figure 3.25(b)). The artificial broadening of interfacial profiles being one of the most common artifacts in AES, it was firstly necessary to check if the profiles were actually representative of the samples. As detailed in section 3.2.2, many precautions were taken in order to limit this artifact:

- A grazing angle of incidence (80 °) was used during the ion bombardment;
- The samples were rotated during milling which enables an averaging of the angle with respect to the crystallographic directions in the sample and thus reduces the ion beam induced roughening. It should be mentioned that the roughening scales with the removed layer thickness and is thus is generally negligible at the beginning of the profiling;
- The applied ion energy was 1 keV which is appropriate for obtaining depth resolution in the range of 1 nm.

Thanks to this setup, the obtained depth resolution on flat interfaces is of 1-2 nm [55-57]. As a consequence, the interface between the Ni and the TiN therefore appears to be composed of an approximately 3 nm thick interlayer where both Ni and TiN inter-diffuse. A similar trend can be observed under the Ni layer where Ni, In, Ga and As co-exist over a depth of approximately 25 nm. It is important to note that the initial substrate stoichiometry is conserved within this interlayer, suggesting that it was formed by the diffusion of some Ni atoms into the InGaAs top surface. As a result, while all interfaces look very flat and sharp on the TEM cross section, interdiffusion is initiated during the deposition of the metallic layers on the InGaAs surface.

Finally, it is worth noticing that contrary to the case of InP surfaces, no amorphous layer is present on InGaAs submitted to Ar^+ plasma pre clean. This observation comes as no surprise as extensive studies conducted in our group highlighted the fact that the InGaAs is way less sensitive to wet and dry surface preparations than InP [51, 58]. Contrary to InP, InGaAs surfaces can therefore be dipped into concentrated HCl solutions (HCl : H_2O = 1 : 2) and submitted to Ar^+ pre clean without being impacted in terms of morphology and / or stoichiometry.

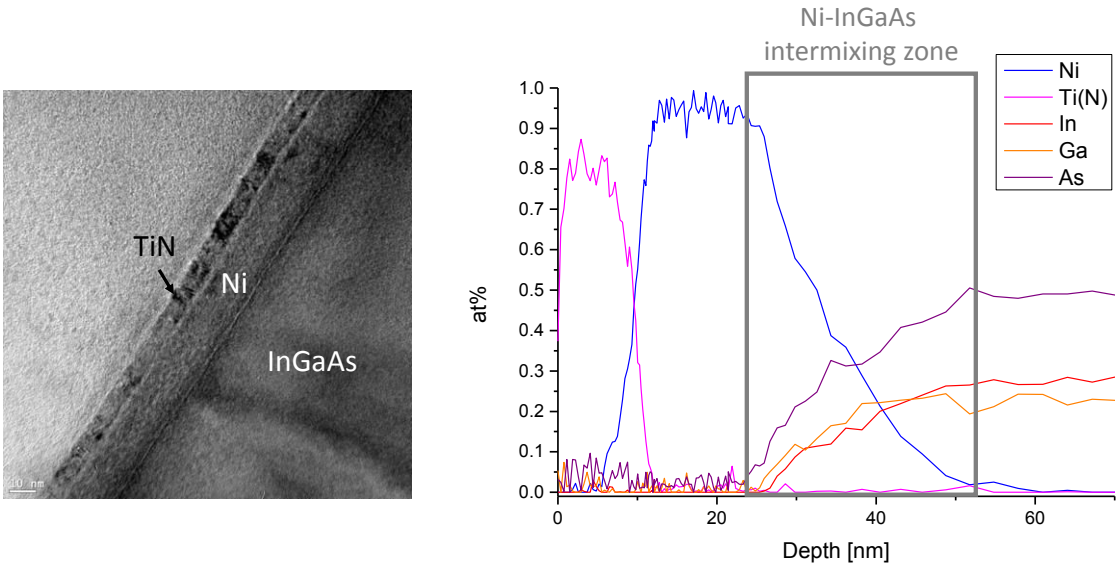


Figure 3.25: (a) TEM and (b) AES characterization of the as deposited TiN (7 nm)/Ni (20 nm)/InGaAs sample.

3.6.2 Analysis of the annealed samples and discussion

After analyzing the as deposited samples, they were annealed thanks to RTP treatments at temperatures ranging from 250 °C to 550 °C for 60 seconds. The resulting systems were first of all characterized by XRD in order to determine the phases in presence. The corresponding XRD patterns are presented in Figure 3.26.

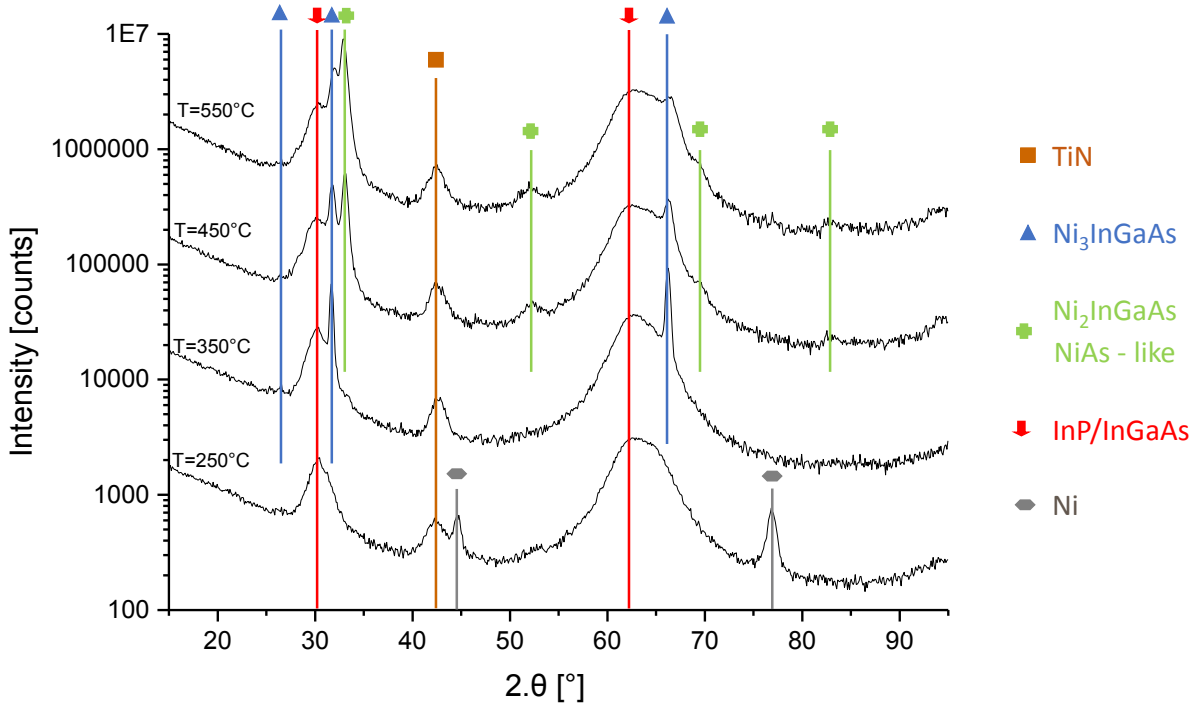


Figure 3.26: θ/2θ XRD patterns of the Ni/InGaAs samples annealed at 250 °C, 350 °C, 450 °C and 550 °C for 60 seconds (RTP). A 2° offset on the incident beam was applied in order to minimize the substrate contribution.

As indicated by the peak indexation, the RTP conducted at 250 °C did not result in the formation of new crystalline phases. At this temperature, the Ni is still the only diffracting species along with the TiN encapsulation. An additional XRR characterization confirmed that the sample is still composed of the deposited 20 nm thick Ni film encapsulated by the TiN (7 nm) at 250 °C. This conclusion is in accordance with the findings of Zhiou *et al* who characterized identical samples thanks to 3D-RSM and highlighted the absence of reaction at this temperature [29]. However, increasing the temperature up to 350 °C resulted in the total consumption of the Ni phase to form new intermetallic compound(s). Unfortunately, the identification of the corresponding diffraction peaks was not enabled by the available Powder Diffraction Files (PDF) as no indexed compound would match the diffracting positions. Nevertheless, as already mentioned in section 3.5, Seifeddine Zhiou reported original results on the Ni/InGaAs system by observing the appearance of the phases $Ni_3In_{0.53}Ga_{0.47}As$, $Ni_2In_{0.53}Ga_{0.47}As$ and NiAs [29, 54]. Thanks to theoretical calculations, the crystallographic parameters along with the theoretical diffracting positions corresponding to these phases were determined[2]. The latter which are summarized in Table 3.6 were used to index the diffractograms corresponding to the annealed samples (Figure 3.26).

[2] As a reminder, in the study reported by Seifeddine Zhiou, while the transition from $Ni_3InGaAs$ to $Ni_2InGaAs$ is accompanied by a modification of the diffracting position (shit > 2 °), the transition from $Ni_2InGaAs$ to the NiAs-like compound is only linked to a small shit (shit < 0.3 °) [29]. As a consequence, the second transition cannot be identified thanks to classical θ/2θ characterizations.

Table 3.6: Theoretically calculated diffracting positions corresponding to the $Ni_3InGaAs$ and $Ni_2InGaAs$ / Ni-As phases

Compound	Crystallographic orientation				
	(100)	**(101)**	**(111)**	**(202)**	**(211)**
$Ni_3(In_{0.53}Ga_{0.47}As)$ **a = 3.85 Å** **c/a = 1.37**	26.71°	31.71°	50.41°	66.25°	77.85°
$Ni_2(In_{0.53}Ga_{0.47}As)$ / NiAs **a = 3.6 Å - 3.70 Å** **c/a = 1.4 – 1.45**	27.81° - 28.44°	32.83° - 33.13°	52.47° - 53.41°	68.83° – 69.53°	81.54° – 83.49°

It appears that the annealing conducted at 350 °C resulted in a total consumption of the Ni which reacted with the InGaAs to form a unique $Ni_3In_{0.53}Ga_{0.47}As$ phase. Increasing the temperature up to 450 °C lead to a partial consumption of this intermetallic compound as indicated by the corresponding peaks' intensity decrease. In the meantime, a new compound corresponding to the $Ni_2(In_{0.47}Ga_{0.53})As$ and/or NiAs-like was formed. This trend is confirmed at 550 °C as this annealing process resulted in further consumption of the $Ni_3In_{0.47}Ga_{0.53}As$ along with the promotion of the $Ni_2(In_{0.47}Ga_{0.53})As$ and/or NiAs-like phases. As a consequence, the indexation of the XRD patterns indicates the formation of $Ni_3(In_{0.47}Ga_{0.53})As$ at 350 °C contrary to most studies which report a unique $Ni_4InGaAs_2$, also noted $Ni_2In_{0.53}Ga_{0.47}As$, phase around this temperature [11-13, 27, 28]. Therefore, in order to further identify the composition of the systems along with their morphology, additional characterizations were conducted on the systems annealed at 350 °C and 550 °C.

Sample annealed at 350 °C for 60 seconds

SEM and TEM lamellae were prepared from the sample annealed at 350 °C for 60 seconds in order to characterize its morphology. The corresponding cross sections are presented in Figure 3.27.

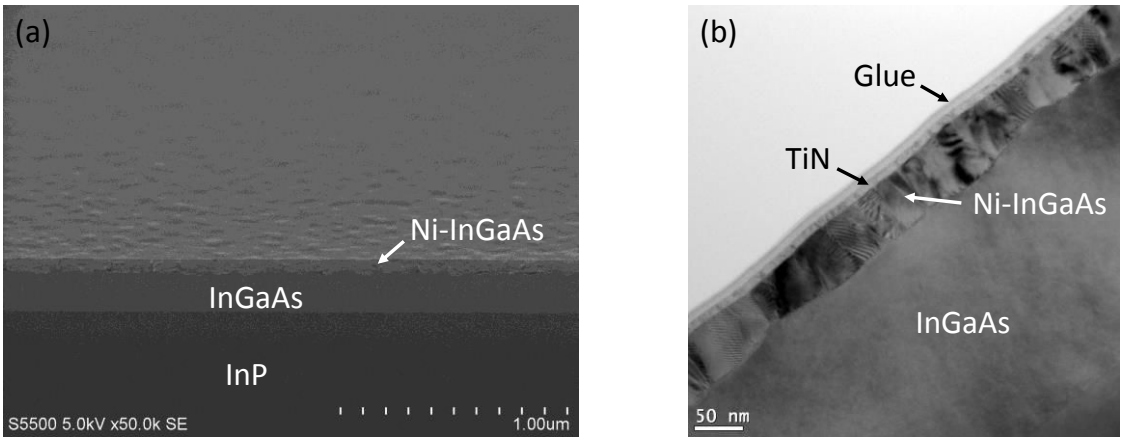


Figure 3.27 (a): SEM and (b) Bright field TEM image of the TiN (7 nm)/Ni (20 nm)/InGaAs sample annealed at 350 °C for 60 seconds.

Both characterizations evidence the presence of a uniform and polycrystalline layer on the InGaAs surface while literature reported an epitaxial relationship between the reaction product and the substrate. The resulting interface is not plane but is determined by the crystallographic orientation of the intermetallic compound's columnar grains. Furthermore, while only 20 nm of Ni were deposited, the thickness of the compound resulting from the reaction of Ni with InGaAs oscillates between 45 and 65 nm. Therefore, contrary to the literature that mainly reported thickness ratio Ni/Ni-InGaAs of about 1.7, it appears to be comprised between 2.2 and 3.2 in our case.

The crystallography of the observed compound was further studied thanks to High Resolution TEM (HRTEM). Both the overall cross section and the Fast Fourier Transform (FFT) corresponding to grain 2 are presented in Figure 3.28. It is important to note that the latter was treated using the method described in [60][3].

[3] The indexation of FFT patterns is similar to that of diffraction patterns. The latter requires the use of the two spots (*i.e.* two reciprocal lattice vectors) that are the closest to the center of the FFT pattern. Clicking on them allows the calculation of their modulus ($|G_{hkl}| = \frac{2\pi}{d_{hkl}}$ where d_{hkl} is the interreticular distance defined in Figure 4.4) and the angle that separates them by the software. Then, suggested individual indexing solutions are proposed based on the results for each diffraction pattern.

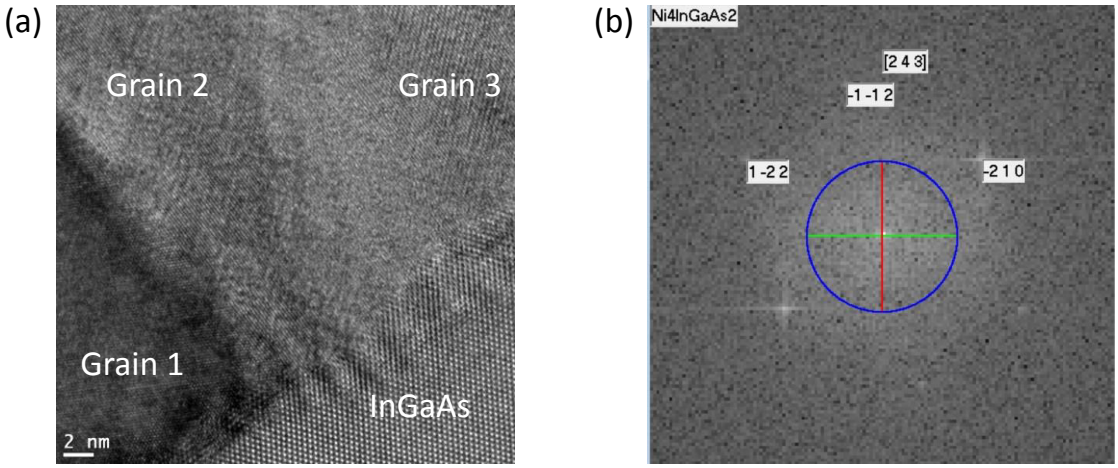


Figure 3.28: (a) HRTEM image of the interface between 3 grains and the InGaAs in the TiN(7nm)/Ni(20Nm)/InGaAs after the 60s-RTP at 350 °C and (b) FFT pattern of grain 2.

Allowing a tolerance on the d value, the FFT pattern was indexed with the crystallographic parameters of the hexagonal $Ni_4InGaAs_2$ phase reported by Ivana *et al* [28]. Although the three observed grains are very differently oriented, all FFT patterns were indexed in the same way. However, having to allow a tolerance on the d parameter most likely reflects the fact that the phase in presence has a crystallographic structure close to that of $Ni_4InGaAs_2$ but is not strictly this phase. Several Ni-InGaAs phases might therefore be arranged along the same crystallographic structure, but present different stoichiometry as it was reported for the Ni/GaAs system. Indeed, Guérin and Guivarc'h demonstrated that all of the ternary Ni-GaAs phases crystallize in comparable hexagonal structures [61, 62]. Therefore, combining this crystallographic characterization with a compositional one appeared to be a necessity in order to determine the exact stoichiometry of the phase. Thus, this sample was characterized thanks to AES and APT measurements which allow a precise identification of the compound's composition.

The corresponding AES profile is presented in Figure 3.29.

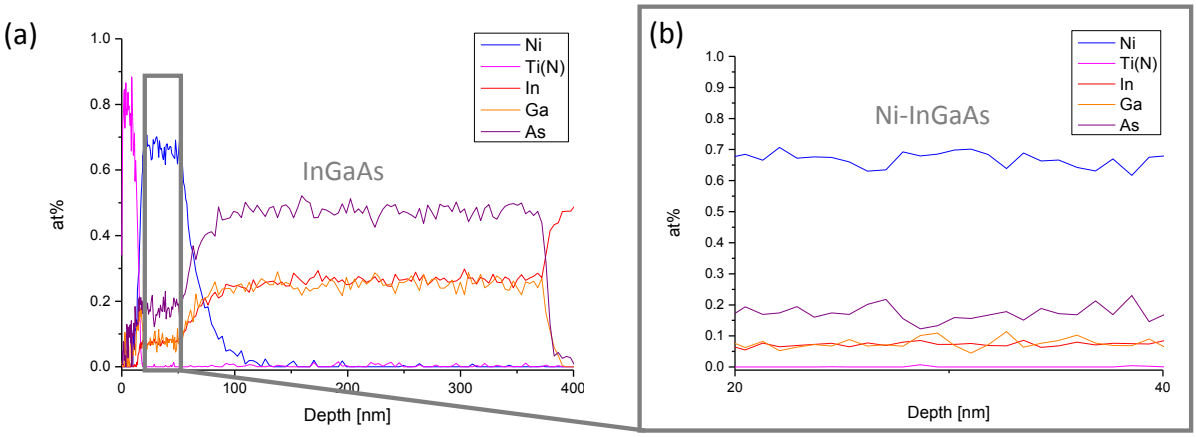


Figure 3.29: (a) AES profile of the TiN(7nm)/Ni(20nm)/InGaAs sample annealed at 350 °C for 60 seconds and (b) zoom on the top of the interfacial reaction zone.

The sample's roughness being very low, the transition between the layers is sharp, therefore enabling a clear identification of the various compounds. Figure 3.29 highlights the presence of a 60 nm-thick intermixed layer containing all the Ni present in the stack. The composition of this layer appears to be homogeneous throughout the depth. However, as hypothesized thanks to the XRD and the FFT indexation, the phase does not seem to correspond to the $Ni_4InGaAs_2$. Indeed, the ratios indicate that the layer's composition is Ni:In:Ga:As = 66:8:8:18, therefore corresponding to the $Ni_3(In_{0.53}Ga_{0.47})As$ phase already observed by Zhiou *et al* at the same temperature.

This conclusion was supported by the APT characterization conducted on a similar sample [59]. It is important to precise that the initial Ni layer thickness had to be brought up to 80 nm to enable this kind of characterization. After conducting the thermal treatment, a tip was made from the sample, evaporated and analyzed. The tip reconstruction is presented in Figure 3.30 along with the corresponding 1D concentration profiles.

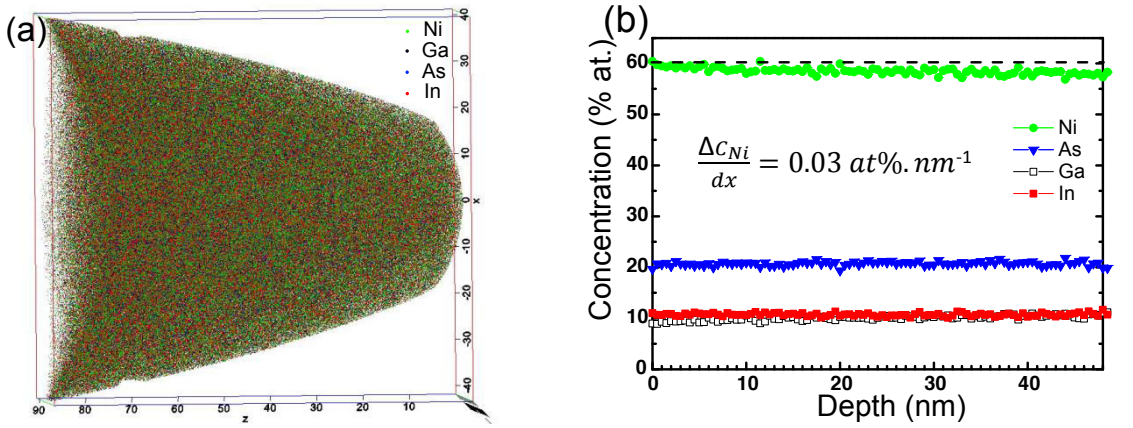


Figure 3.30: (a) Reconstructed 3D volume and (b) corresponding 1D profile showing the at % along the depth of the TiN(7 nm)/Ni(20 nm)/InGaAs sample annealed at 350 °C for 60 seconds.

The reconstructed 3D volume exhibits a uniform composition that was deduced from the mass spectrum as explained in section 3.2.2. The chemical composition averaged over the whole volume is 58.6 at% Ni, 20.9 at% As, 11.0 at% In and 9.5 at% Ga. Therefore, the phase identified thanks to APT appears to be $Ni_3(In_{0.53}Ga_{0.47})As$ which indicates that the nominal proportions of In, Ga and As of the substrate are kept in the reaction product. This observation suggests the fact that, as reported in the literature, the Ni-InGaAs intermetallic compound is formed thanks to the diffusion of Ni atoms. The corresponding 1D profile extracted from a cylindrical region perpendicular to the interface and having a diameter of 30 nm is presented in Figure 3.30(b). The latter highlights a non-negligible Ni gradient, *i.e.* 0.03 at%.nm^{-1}, which is compensated by an inverse Ga gradient along the depth of the intermetallic compound. Because Ni and Ga atoms do no occupy the same crystallographic positions, this suggests the fact that the $Ni_3(In_{0.53}Ga_{0.47})As$ accepts a stoichiometry deviation. Even though the overall phase appears to be uniform, the In atoms present a non-homogeneous distribution as depicted in Figure 3.31. Contrary to the Ni, Ga and As atoms, the In is accumulated on the grain boundaries (GB). This accumulation might not be significant at this temperature but might become problematic with the increase of temperature. Indeed, if this phenomenon is heightened it might result in the formation of the In phase as it was observed in the Ni/InP system which may lead to a performance variability of the contacts.

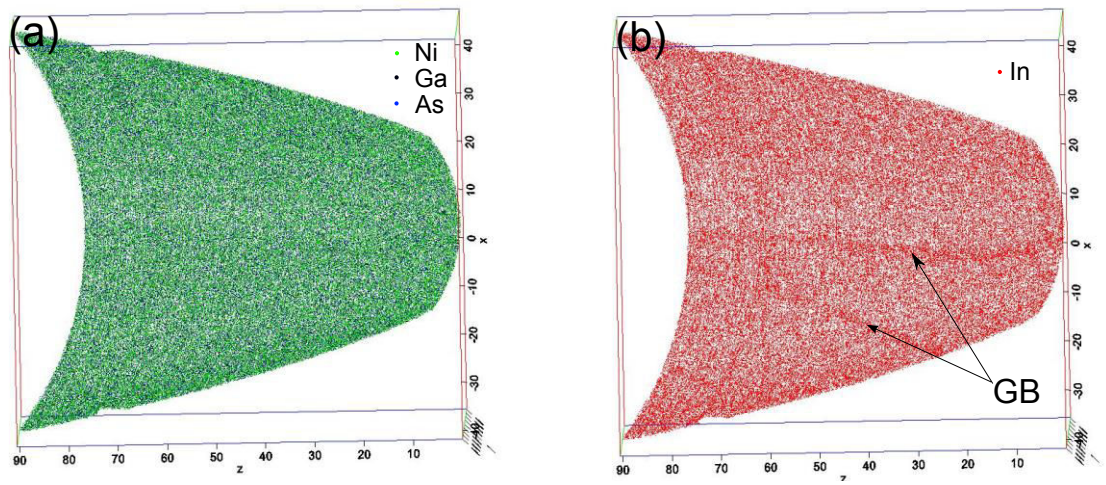


Figure 3.31: Cross sectional view of a 10 nm-tick slice (xz plane) extracted from the 3D volume showing the distribution of (a) the Ni, Ga and An and (b) the In.

In conclusion, every compositional characterization conducted on the Ni/InGaAs system annealed at 350 °C for 60 seconds highlighted the presence of a uniform hexagonal $Ni_3(In_{0.53}Ga_{0.47})As$ phase. This phase could be indexed as the $Ni_4InGaAs_2$ on the SAED pattern because the crystallographic arrangements of the two phases are very close from one another. Both of them crystallize under a B8 hexagonal structure as reported by Ivana *et al* and Zhiou *et al* [28, 29].

Sample annealed at 550 °C for 60 seconds

The highest thermal budget applied on the Ni/InGaAs system corresponds to a 60 seconds treatment at 550 °C. Because such a high temperature might have undesirable effects on the morphology and the chemistry of the system, it was firstly characterized by SEM and TEM (Figure 3.32).

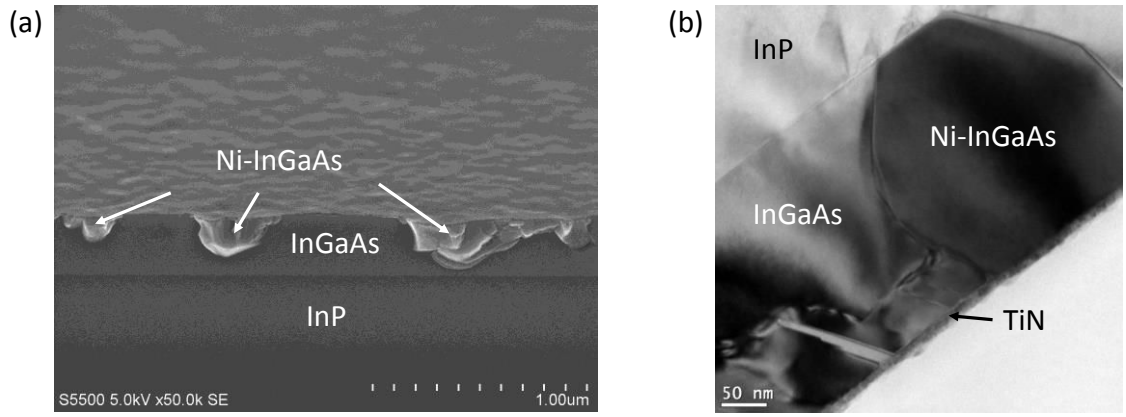


Figure 3.32: (a): SEM and (b) Bright field TEM image of the TiN (7 nm)/Ni (20 nm)/InGaAs sample annealed at 550 °C for 60 seconds.

The corresponding cross sections highlight a pronounced agglomeration of the film. While the film was initially 20 nm thick, the agglomerates reach depths of a few hundreds of nanometers. The biggest ones, as featured by Figure 3.32(b) even reach the bottom of InGaAs epitaxy, *i.e.* the carrier InP substrate. In order to determine the localized repartition of the elements in the grains and in the surrounding areas, EDS measurements were performed (Figure 3.33).

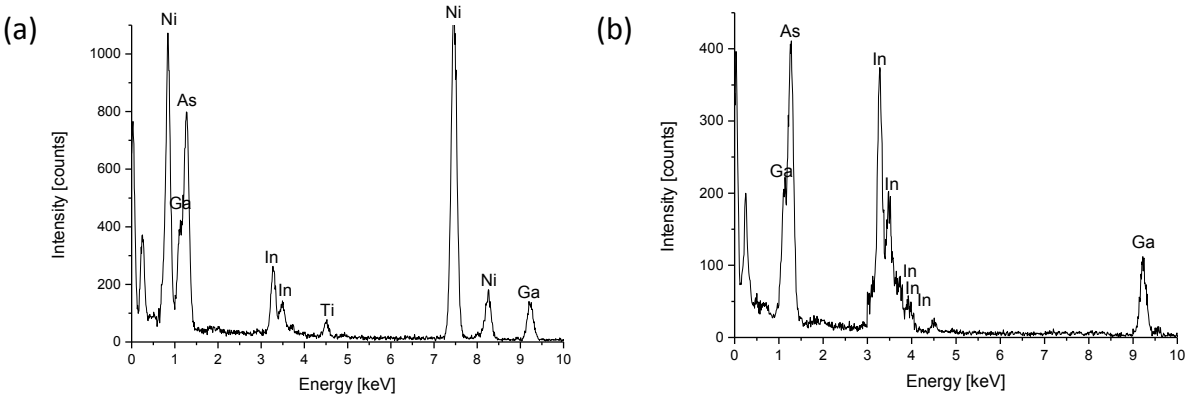


Figure 3.33: EDS characterization of (a) agglomerates and (b) surrounding areas present in the TiN(7nm)/Ni(20nm)/InGaAs sample annealed at 550 °C.

The latter indicate that the integrality of the Ni present in the system is contained in the agglomerates while the surrounding areas are composed of pure InGaAs. In order to characterize more precisely the composition of these agglomerates, additional AES and APT characterizations

were conducted at this point. However, the important inhomogeneity of the sample resulted in an averaging of the signals emanating from the various regions therefore hindering the treatment of the AES data. As a consequence, only the results extracted from the APT experiment will be presented in the following.

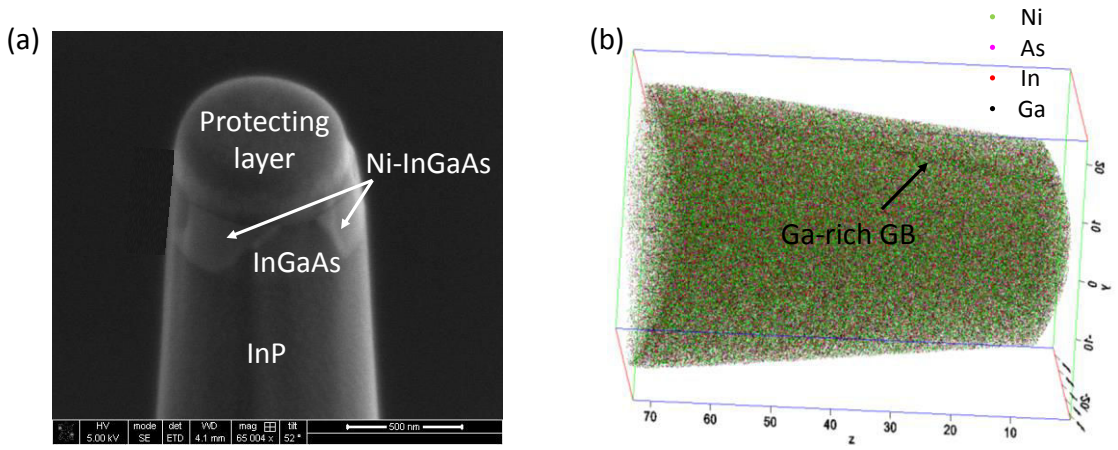


Figure 3.34: (a) SEM image of the APT tip fabricated from the TiN(7nm)/Ni(20nm)/InGaAs sample annealed at 550 °C and (b) 3D reconstructed volume of a region containing only the Ni-InGaAs compound.

The SEM image of the fabricated tip is shown in Figure 3.34(a). One can observe the Ni-InGaAs agglomerates surrounded by the InGaAs at the top of the tip. The reconstructed 3D volume corresponds to a zone containing only the Ni-InGaAs compound and displays a uniform repartition of the atoms in the phase present at this temperature. Only one singularity corresponding to a Ga-rich grain boundary can be observed in the whole tip. The overall composition determined from three different experiments is Ni:In:Ga:As = 52:12:4:32. Therefore, it appears that almost no Ga is present in the compound which is mainly Ni and As-rich. This finding is in accordance with the study of Zhiou *et al* who report the formation of a NiAs-like phase at 550 °C.

3.6.3 Summary of the results

In conclusion, it appears that the as deposited Ni/InGaAs is not modified by an annealing treatment conducted at 250 °C for 60 seconds. However, increasing the temperature up to 350 °C is sufficient to cause the total consumption of the Ni and the formation of a unique and uniform $Ni_3(In_{0.53}Ga_{0.47})As$ phase. Allowing a tolerance, the latter can be indexed using the crystallographic parameters of the $Ni_4InGaAs_2$ phase reported by Ivana *et al* as both phases are arranged in a B8 hexagonal structure [28, 29]. At 550 °C however, the Ni-containing compound is fully agglomerated and depleted in Ga and In. The phase formed at this temperature corresponds to a NiAs-like phase containing a small amount of In and Ga. In spite of this drastic change of stoichiometry, the crystallographic structure is

not modified during the annealing treatments conducted at various temperatures and is still hexagonal.

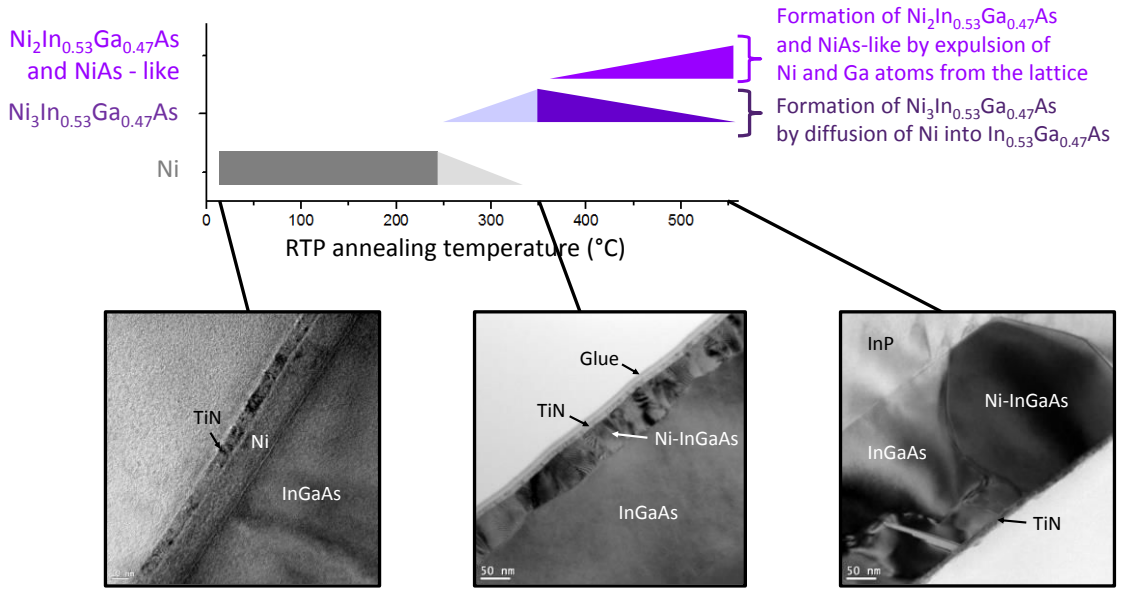


Figure 3.35: Summary of the metallurgical study conducted on the Ni/InGaAs system. The light fillings correspond to temperatures that were not investigated and for which only trends on the phases' evolution are displayed.

3.7 State of the art about Ti-based metallizations on InP

Ti is a widely used metal in the classical Ti/Pt/Au contacts both on n- and p-type semiconductors where it provides the primary role of improved metallization adhesion. As a result, Ti is the metal in contact with the semiconductor and mainly rules the electrical properties of these contacts. Therefore, in the scope of forming noble materials-free contacts, Ti was more particularly studied on its own.

Persson *et al* report the initiation of a reaction during the Ti deposition [15]. Although no binary or ternary crystalline phase was detected by XRD at this point, some In was released probably indicating the formation of Ti-P phases. They did not observed any modification at 250 °C but strong diffraction signals from TiP were observed at 350 °C. The diffraction patterns indicated the presence of TiP and In up to 600 °C, where TiP is the dominating compound. The authors conclude that the formation of the TiP phase is initiated at low temperatures and that this compound acts as a diffusion barrier which inhibits further reaction afterwards. Therefore, even at 500 °C, the reaction seems incomplete.

A similar phase sequence is observed by Takeyama *et al* who identified the presence of an intermixed Ti-P layer along with some In release after the Ti deposition [9, 63]. The authors found out

that the intermixed layer is converted into stable binary Ti-P compounds after annealing treatments from 300 °C to 600 °C. The latter is associated with some In outdiffusion and segregation, therefore leading to a Ti/In/Ti-P/InP stack. However, they do not precise the nature of the binary Ti-P phase which could be composed of TiP or Ti_4P_3 according to them. This founding agrees with that of Wang and Ivey (see below) except for the behavior of the segregated In atoms that are piled up at the Ti-P/InP interface in their study [64]. The authors attribute this difference to the fact that their system was capped with an Al layer contrary to that of Wang *et al* where the uncapped Ti layer is directly affected by the oxidation.

Kendelewicz *et al* studied more particularly the reactions occurring during the Ti deposition at room temperature and showed the initiation of the reaction after the deposition of only 0.2 Å of Ti [65]. They highlighted the formation of a Ti-In alloy along with two different Ti-P phases, without further detail on the composition of the phases. At higher coverage, In is found to outdiffuse and segregate in the reaction product (t ≤ 18 Å) before being diluted (t > 18 Å). Chassé *et al* conducted a similar study and also showed that the formation the TiP phase is initiated during the deposition process, without any critical minimum coverage. This reaction is associated with removal of In from the substrate which arranges in metallic form in the surface region and/or in the reacted layer. When the deposition is carried on (t > 19 Å), the In is diluted in the reacted compound and a Ti layer grows on top of it, probably in the form of islands. This indicates that the TiP acts as a diffusion barrier which inhibits further formation of the reaction products. Additional studies conducted on annealed samples highlighted a broadening of the reaction product from 150 °C along with a consumption of the Ti.

On the contrary, Wang and Ivey [64] did not analyze the as deposited sample but identified the first signs of reaction at 325 °C while lower temperatures were probed. At this temperature, they identified two different regions at the Ti/InP interface, *i.e.,* an In-rich region and a region containing Ti and P. At 350 °C, they identified the phases in presence, leading to the following stack: Ti/Ti-P/In/InP. Again, based on Selected Area Diffraction (SAD) data, the authors mention the fact that the Ti-P containing layer could actually be composed of TiP, Ti_4P_3 or a combination of both phases. From their findings however, even if both phases coexist, the TiP appears to be predominant. A similar characterization conducted after a thermal treatment at 450 °C for 1.5 hours allowed the identification of the phase as TiP. Increasing the temperature also lead to a decrease of the In layer's thickness which is found to diffuse at the top of the stack where it is oxidized. This In_2O_3/Ti/TiP/In/InP stack appears to be stable up to temperatures as high as 550 °C.

The phase sequences reported in these studies are summarized in Table 3.7.

Table 3.7: Non exhaustive recapitulative table of the phase sequences observed in the literature - Ti/InP system (When encountered, N/A stands for Not Available)

Ni Thickness	Surface preparation	Deposition technique	Annealing ambient	Annealing temperature and duration	Observed compounds	Reference
50 nm	N/A	E-beam evaporation	Vacuum at 1.3×10^{-5} Pa	As deposited	Crystalline Ti + In Presence of P	[15]
				250 °C – 30 min		
				350 °C – 30 min	Crystalline Ti + TiP Presence of In	
				400 °C – 30 min	Crystalline TiP + In Presence of Ti	
				450 °C – 30 min		
				550 °C – 30 min		
50 nm	HF:H_2O=1:5 for 1 min	DC Sputtering	N_2	As deposited	Ti/In/Ti-P/InP	[9, 63]
				300 °C – 20 s		
				500 °C – 20 s		
				600 °C – 20 s		

Ni Thickness	Surface preparation	Deposition technique	Annealing ambient	Annealing temperature and duration	Observed compounds	Reference
t < 19 Å	N/A	Evaporation (1 to 3 Å/min)	N/A	As deposited (t < 19 Å)	In/Ti-P/InP	[66]
t = 20 Å				As deposited (t > 19 Å)	Ti/In/Ti-P/InP	
				100 °C – 5 min	Ti/In/Ti-P/InP	
				150 °C - 5 min	(Ti)/In/Ti-P/InP	
				200 °C – 5 min		
				250 °C – 5 min		
120 nm	N/A	E-beam evaporation	Forming gas (95% N_2 + 5% H_2)	As deposited	Ti/Oxide/InP	[64]
				325 °C – 5 min	In_2O_3/Ti/TiP/In/InP	
				350 °C – 2 hours		
				450 °C – 1.5 hour		
				550 °C		

3.8 Metallurgical study of Ti-based metallizations on InP

3.8.1 Analysis of the as deposited samples

After the wet and dry surface preparations conducted respectively in a concentrated HCl solution and under an Ar^+ plasma, the 20 nm-thick Ti films were deposited at 100 °C and were capped by a TiN layer (7 nm) deposited at the same temperature. In order to determine the composition of the systems, the samples were firstly analyzed thanks to XRD detexturation. Several Ti thicknesses ranging from 20 nm to 50 nm were probed as displayed in Figure 3.36.

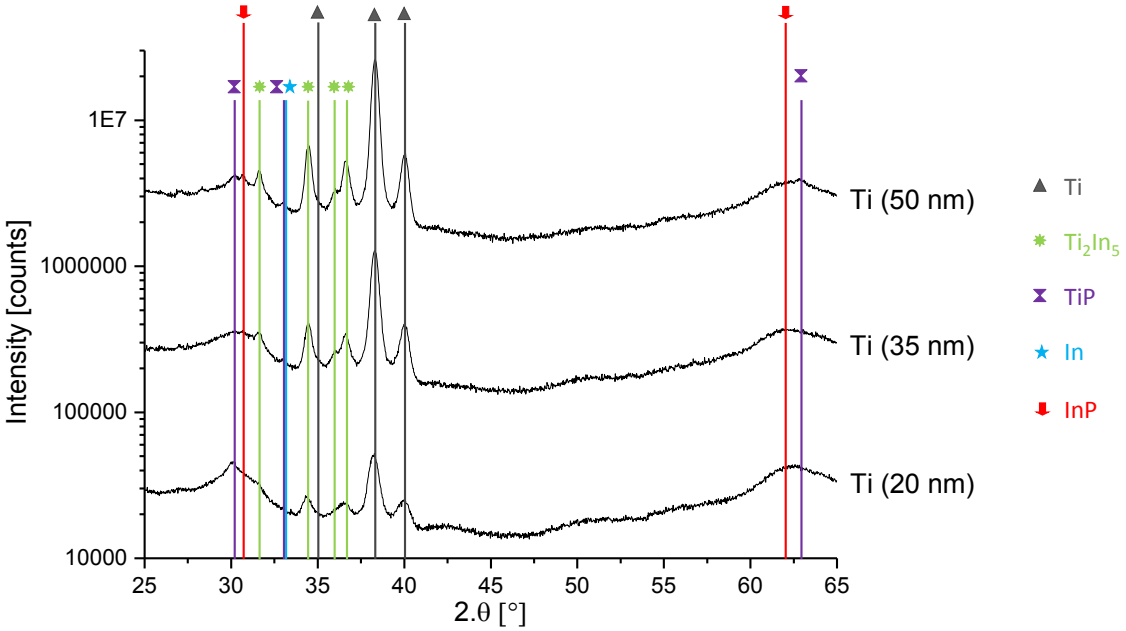


Figure 3.36: XRD detexturation pattern of the as deposited TiN (7 nm)/Ti (20 nm, 35 nm and 50 nm)/InP samples.

In accordance with most results reported in literature, the XRD patterns highlight the initiation of the reaction between Ti and InP during the deposition process [9, 15, 63, 65, 66]. This reaction appears to be incomplete as several peaks corresponding to the Ti are still observed, even when only 20 nm of metal were initially deposited. The XRD patterns highlight the formation of at least two binary and crystalline phases, the hexagonal TiP and the tetragonal Ti_2In_5. While the formation of the first phase is largely reported in literature, the second has not been observed yet. It is important to note that some In might also be present in these systems as one peak might be attributed to this phase ($2\theta = 33°$). However, this assumption could hardly be affirmed solely thanks to the XRD as this peak could also be attributed to TiP. Therefore, in order to identify more precisely the nature and the

repartition of the various phases, additional TEM combined with AES characterizations were conducted on the TiN(7 nm)/Ti(20 nm)/InP and TiN(7 nm)/Ti(50 nm)/InP systems.

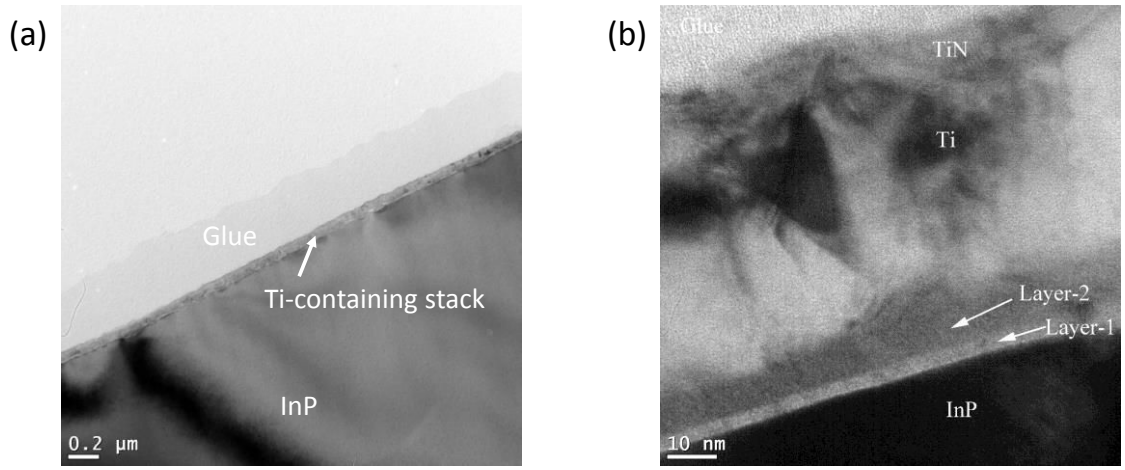


Figure 3.37: Bright field TEM cross section of (a) the TiN(7 nm) / Ti (20 nm) / InP sample in low magnification and (b) the TiN(7 nm) / Ti (50 nm) / InP sample in high magnification highlighting the presence of four different layers in the system.

The low magnification TEM images highlight the homogeneity and the continuity of the layers present on the InP (Figure 3.37(a)). Increasing the magnification reveals the presence of two different layers underneath the Ti whose grains are about 40 nm wide (Figure 3.37(a)). Although both layers' thicknesses are not perfectly homogeneous within each system, they are independent from the initially deposited Ti thickness:

- The thickness of layer 1 ranges from 3 nm to 8 nm within each sample;
- The thickness of layer 2 ranges from 7 nm to 15 nm within each sample.

Additional AES characterizations were conducted in order to determine the composition of both layers. Because they are very similar, Figure 3.38 displays solely the results corresponding to the system TiN(7 nm) / Ti (20 nm) / InP.

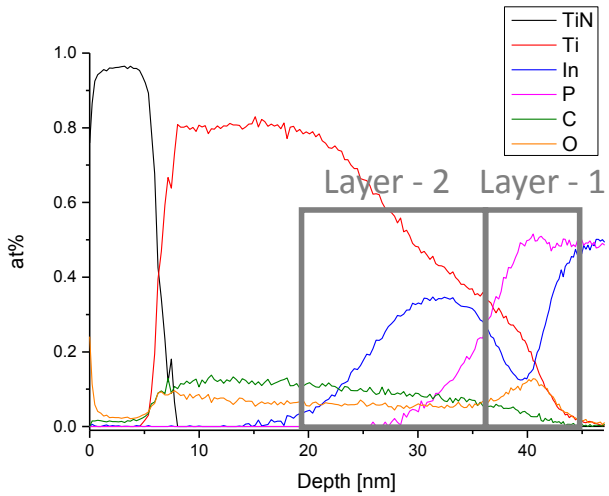


Figure 3.38: AES profile corresponding to the as deposited TiN(7 nm)/Ti(20 nm)/InP system.

As supported by the AES profile, the two layers present very different compositions. While the layer in contact with the Ti (layer – 2) is composed of a mixture of Ti and In, the layer in contact with the InP (layer – 1) is comprised of Ti and P. By linking these results with the XRD characterization, one must reasonably assume that these two layers are respectively composed of Ti_2In_5 and TiP. As a consequence, the Ti reacts with the InP during the deposition process conducted at 100 °C to form the layered structure: TiN(7 nm)/Ti/Ti_2In_5(7 nm to 15 nm)/TiP(3 to 8 nm)/InP.

3.8.2 Analysis of the annealed samples

In order to determine the evolution of the structure identified after deposition, additional characterizations were conducted on samples annealed thanks to RTP processes at temperatures ranging from 250 °C to 550 °C. The XRD detexturation patterns corresponding to these samples are presented in Figure 3.39 and Figure 3.40 respectively for initial Ti thicknesses of 20 nm and 50 nm.

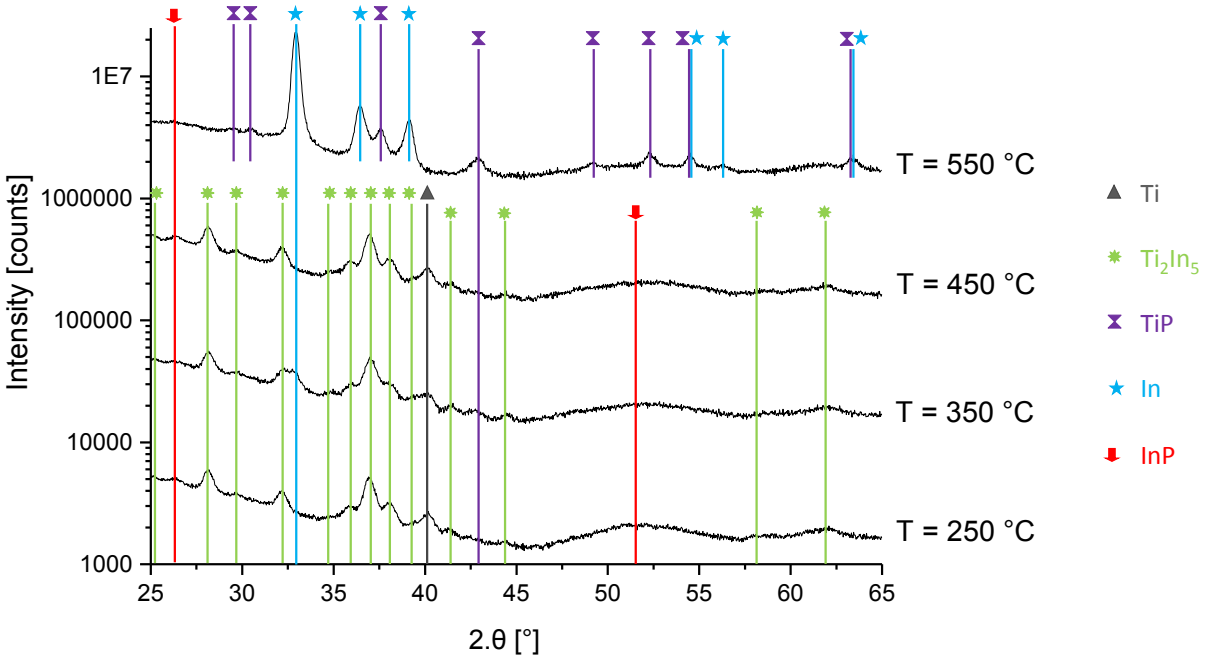


Figure 3.39: XRD detexturation patterns of the TiN (7 nm)/Ti (20 nm)/InP samples annealed at 250 °C, 350 °C, 450 °C and 550 °C for 60 seconds (RTP). A 2° offset on the incident beam was applied in order to minimize the InP substrate contribution.

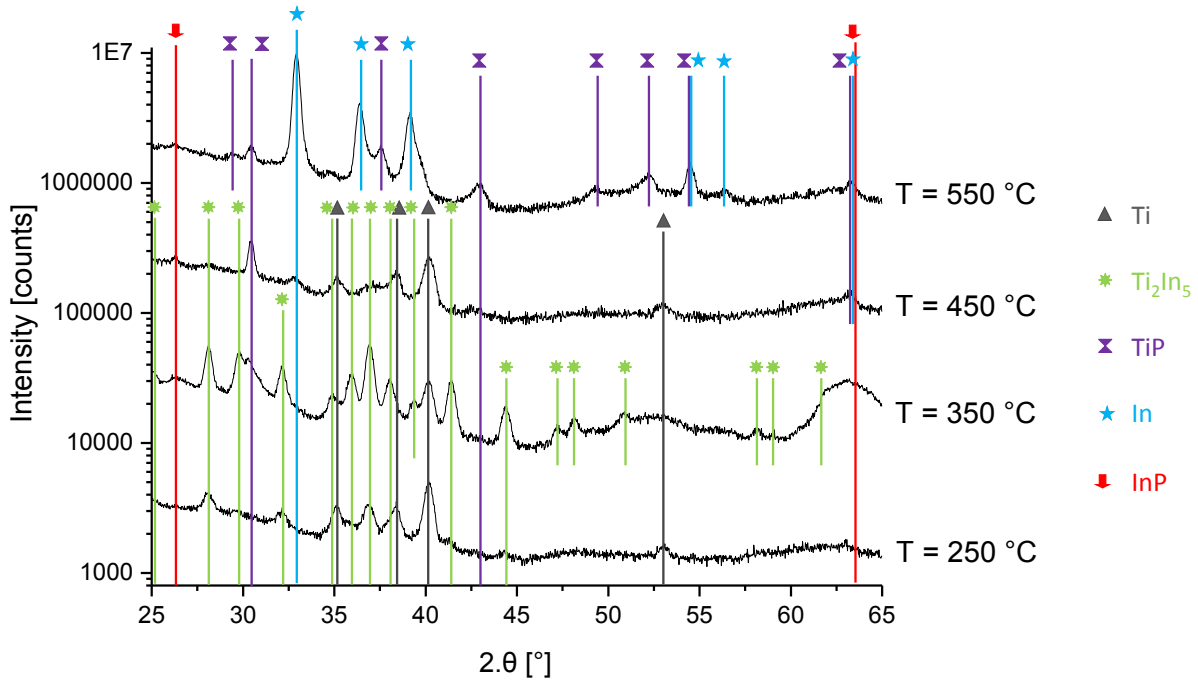


Figure 3.40: XRD detexturation patterns of the TiN (7 nm)/Ti (50 nm)/InP samples annealed at 250 °C, 350 °C, 450 °C and 550 °C for 60 seconds (RTP). A 2° offset on the incident beam was applied in order to minimize the InP substrate contribution.

When only 20 nm of Ti are initially deposited, the diffractograms highlight the coexistence of the three phases already observed, *i.e.,* Ti, Ti_2In_5 and TiP, at temperatures up to 450 °C (Figure 3.39). Furthermore, the intensity of every diffraction peak is constant throughout the annealing temperatures and, thus, do not indicate the evolution of the phases in this range. However, increasing the initial Ti thickness leads to a modification of the peaks' behavior (Figure 3.40). Indeed, peaks corresponding to the Ti_2In_5 and the TiP are not present on all the samples, and most importantly seem to disappear at some temperatures. For example, one of the most intense TiP peak ($2\theta = 30.3°$) is absent at 250 °C while the XRD conducted after deposition and at higher temperatures indicate the presence of this compound in the corresponding systems. Similarly, all the peaks corresponding to the Ti_2In_5 at angles ranging from 45° to 65° are absent on the patterns acquired after annealing treatments conducted at 250 °C and 450 °C while they are present at 350 °C. Therefore, the extinction of some peaks seems to be uncorrelated with the actual composition of the systems and may be attributed to the crystallographic texture of these compounds. Indeed, even though diffractograms were acquired at several χ angles to give rise to the summed patterns presented above, no rotation was performed around the φ angle in this configuration. Therefore, some orientations might be extinguished depending on the initial positioning of the sample / wafer with respect to the X-Ray beam. In order to confirm or deny this hypothesis, TEM and AES characterizations were conducted on the system presenting an initial Ti thickness of 50 nm annealed at 450 °C (Figure 3.41).

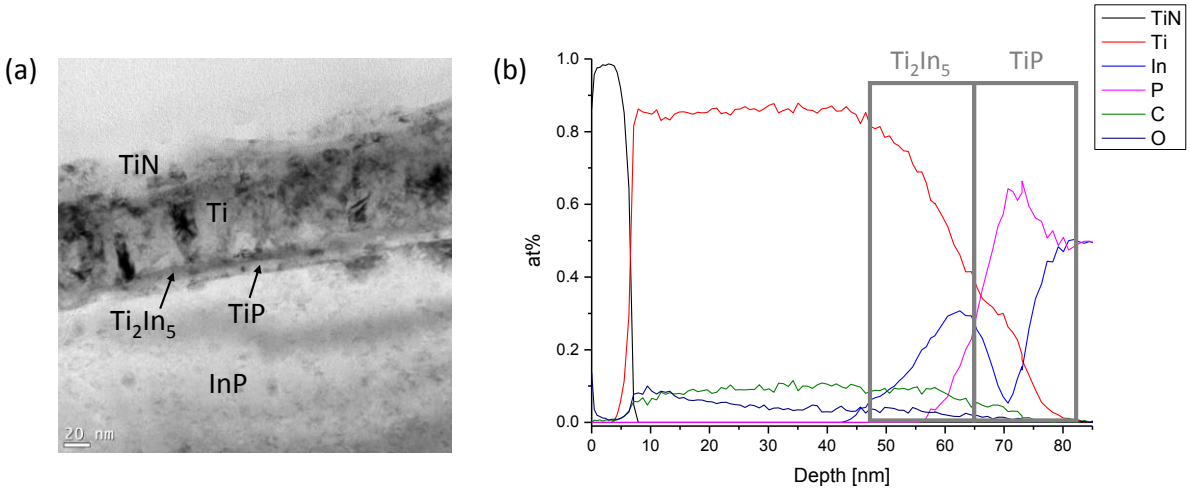


Figure 3.41: (a) TEM cross section of the TiN(7nm)/Ti(50nm)/InP system annealed at 450 °C and (b) corresponding AES profile.

The TEM cross section along with the AES profile feature the presence of four distinct layers which are very similar to the ones observed after deposition in terms of morphology and thicknesses. The Ti-P layer in contact with the InP substrate is still about 3-8 nm thick while the thickness of the Ti-In

layer still ranges from 7 nm to 15 nm[4] . Although the roughness seems to be increased by this thermal treatment, the various compounds are still arranged in the layered structure already observed after deposition: TiN(7 nm)/Ti/Ti_2In_5(7 nm to 15 nm)/TiP(3 to 8 nm)/InP. As a consequence, the modification of the diffractograms from 250 °C to 450 °C is most likely linked to a texture of the observed compounds rather than to an actual modification of the systems' composition. For initially deposited Ti thickness ranging from 20 nm to 50 nm, the TiP and the Ti_2In_5 are formed during the deposition process and are stable in terms of composition and thicknesses at temperatures as high as 450 °C.

However, contrary to the observations made in this range of temperature, a drastic change of composition is brought by an increase of the temperature to 550 °C. At this point, a complete redistribution of the species present in the sample lead to the total consumption of the Ti and of the Ti_2In_5. The latter are replaced by the already observed TiP phase. The stoichiometry conservation leads to some In release as confirmed by the corresponding XRD patterns.

3.8.3 Discussion

In the previous section, thanks to the combined results emanating from XRD, TEM and AES, the composition of Ti(20 nm to 50 nm) / InP systems was determined from deposition temperature to 550 °C. It was found that a layered structure composed of Ti, Ti_2In_5 and TiP is formed during the deposition process conducted at 100 °C and is stable up to 450 °C. However, further increasing the temperature up to 550 °C leads to a consumption of the Ti and the Ti_2In_5 to promote the TiP and In.

The initial appearance of Ti-In phases along with Ti-P phases has not been reported yet in this kind of systems. Because it might modify their electrical properties or their thermal stability, the phenomena responsible for the appearance of the Ti_2In_5 are worth identifying. Similar discrepancies observed on other systems such as the Ni/InP where extensively discussed in the literature and several hypothesis were provided. For example, Appelbaum *et al* and Fatemi *et al* did not report the formation of the same stable compound on the InP substrate after annealing treatments. However, the authors explained that this difference is only an apparent one as it is due to different AES data treatments. In our case, the identification of the phases could hardly be questioned as a multitude of diffracting peaks confirms the indexation of each phase in Figure 3.39 and Figure 3.40.

[4] Note that the roughness present in this system results in transitions that are less net on the corresponding AES profile. As a consequence, the layer's thicknesses are somewhat overestimated on this profile compared to the ones actually measured on the corresponding TEM cross sections and presented in this section.

However, as detailed in in section 3.2.1, all samples were dipped into a concentrated HCl solution and subjected to an Ar^+ pre clean before the metallization deposition in order to remove the native oxides and contaminants from the InP surface. Extensive studies concerning the effect of these surface preparations showed that both treatments modify the InP surface's stoichiometry (see section 3.4.2). Therefore, next section will be dedicated to the study of the observed phase sequence and to the presentation of the mechanisms responsible for the appearance of each observed phase.

Mechanisms involved in the phase sequence

As mentioned in the previous sections, the samples systematically undergo two types of surface preparation, both of them leading to a modification of the initial InP stoichiometry. In order to further understand the individual effect of both the wet and the dry preparation, additional characterizations were conducted. A sample was thus prepared suppressing the Ar^+ pre clean and then characterized thanks to XRD (Figure 3.42). Note that although the suppression of the wet surface preparation would seem relevant from a theoretical perspective, in practice it would lead to unwanted phenomena. Indeed, it would result in the presence of a thick native oxide layer which would inhibit any kind of reaction between the Ti and the InP. As a consequence, Figure 3.42 displays the XRD detexturation corresponding to samples with an initial Ti thickness of 20 nm which did and did not undergo an Ar^+ pre clean treatment.

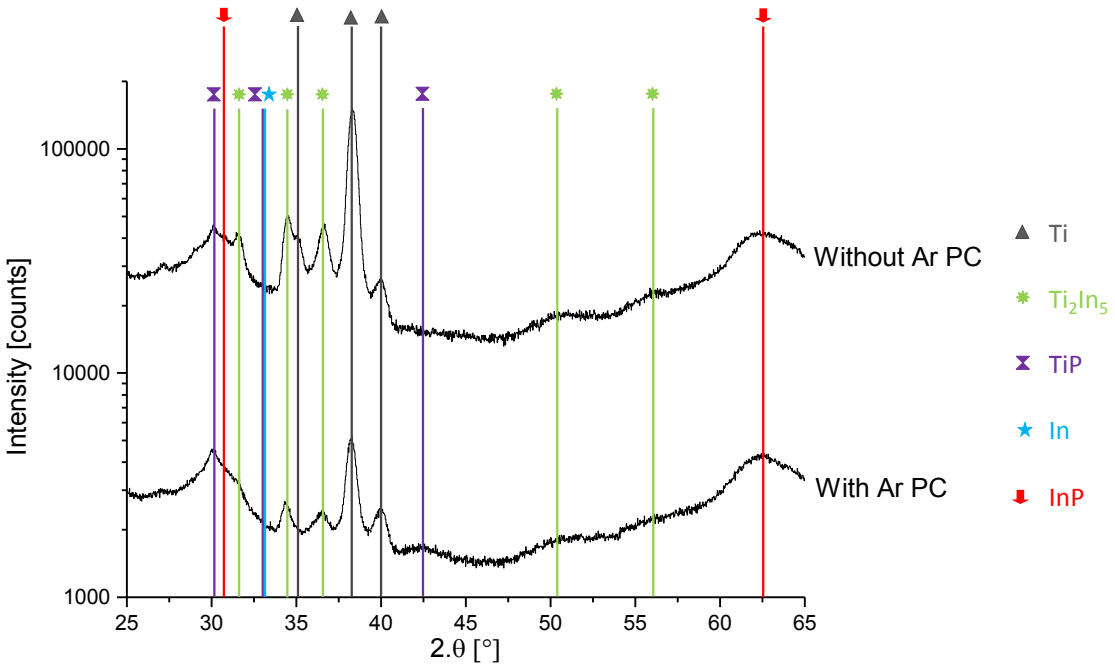


Figure 3.42: XRD detexturations of the as deposited TiN(7 nm)/Ti(20 nm)/InP sample with and without Ar^+ preclean.

The XRD detexturations highlight the formation of the two already observed phases, *i.e.* TiP and Ti_2In_5, both in the presence and in the absence of the Ar^+ pre clean. Therefore, it appears that suppressing solely the Ar^+ preclean is not sufficient to modify the observed phase sequence. However, in accordance with literature, we showed in section 3.4.2 that the concentrated HCl used for the wet surface preparation anisotropically etches the InP leaving the surface In-rich [52]. During the subsequent Ti deposition which is conducted by PVD, the atoms are deposited on this modified surface. A non-negligible portion of the atoms also reaches the InP situated below this In-rich layer either thanks to their kinetic energy and/or thanks to a diffusion process. The compositional gradient present in the InP leads to the formation of two distinct layers, the Ti_2In_5 in the In-rich region and the TiP below. This situation is schematically represented in Figure 3.43.

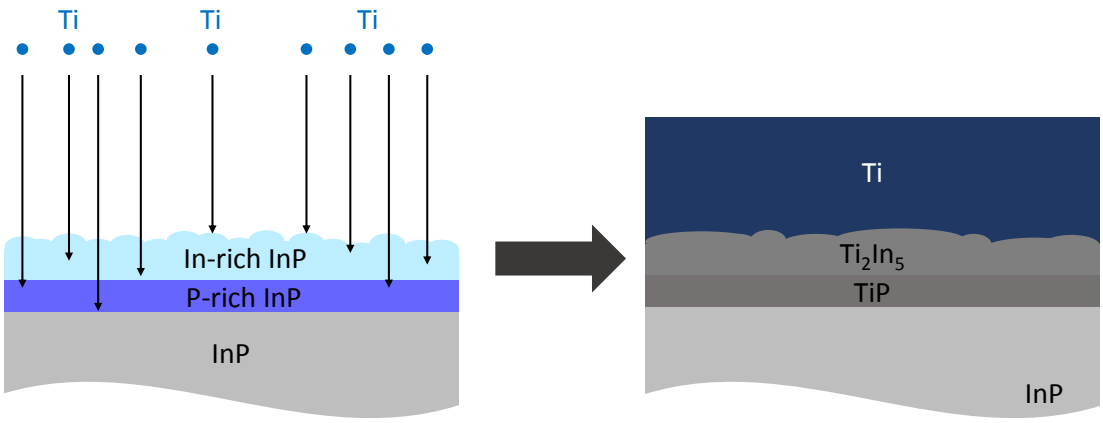


Figure 3.43: Schematic representation of the formation of the Ti_2In_5 and TiP phase during the deposition process.

In order to identify more precisely the involved mechanisms, one must additionally consider the results presented in literature. In most studies, no extensive details are given concerning the surface preparation, with the exception of Takeya *et al* who dipped their InP substrates into HF solutions [9, 63]. It is therefore consistent to assume that the InP surfaces used in these studies have not been modified and are thus composed of 50 at% of In and 50 at% of P. As a consequence, it appears that when the InP surface's stoichiometry is not modified, the formation of Ti-P phases is favored at temperatures as low as 20 °C. This observation leads to two conclusions:

(i) The gain in free energy (ΔG_V) associated to the formation of TiP on unmodified InP is so important that it compensates the increase of surface energy (σ) linked to the nucleation of the phase at temperatures as low as 20 °C (see section 3.1.3). Therefore, the formation of this compound is not limited by the nucleation on intact InP and is thermodynamically favorable on this kind of surface.

(ii) The overall gain in free energy (ΔG_n) associated to the formation of TiP when Ti and unmodified InP are brought in contact is more important than the one associated to the formation of Ti_2In_5. Note

that ΔG_n takes into account the gain in free energy associated to the formation of the binary phase (ΔG_V) and the surface energy required to form the new interfaces (σ).

On the other hand, when the InP surface is modified by the surface preparation and becomes In-rich, these considerations are no longer verified. The kinetic energy due to the PVD deposition bring Ti atoms close to / into the modified layer. In this case, even if the free energy gain would have been maximized by forming the TiP phase, the Ti_2In_5 phase is favored because of the available In excess. Just like TiP, the gain in free energy associated to the formation of Ti_2In_5 compensates the surface energy required to form the nuclei at temperatures as low as 100 °C. The appearance of this phase is therefore not limited by the nucleation process. However, because the TiP phase is thermodynamically more stable on intact InP surfaces, the system tends to form this phase in the regions where the nominal InP stoichiometry is conserved, *i.e.*, below the top few InP nanometers. The formation of Ti-P phases is even more favored in the present case as a P-rich region is present right below the In-rich layer (see Figure 3.14.F). These mechanisms are in accordance with the layered structure which is observed, where the P-rich phase lays below the In-rich one. Furthermore, the formation of the Ti_2In_5 and TiP must occur simultaneously. The P release associated to the appearance of the Ti_2In_5 therefore helps the formation of the TiP; similarly, the In released during the formation of the TiP is at least partially consumed to form the Ti_2In_5. Once continuous TiP and Ti_2In_5 layers are formed, at least one of them acts as a diffusion barrier (bulk and / or grain boundary diffusion) therefore inhibiting further reaction up to 450 °C. It is important to note that even though both layers can inhibit the diffusion, based on literature, the TiP probably plays the most important role. Additionally, P-free “pockets” are observed below the TiP layer as displayed in Figure 3.44. One can reasonably assume that these pockets appear during the formation of the TiP layer. As mentioned above, when the Ti and the InP react together to form the TiP, some In must be released. A certain proportion of the In participates to the formation of the Ti_2In_5 provided that it is not blocked by the TiP diffusion barrier. However, the proportion of In that is released underneath this TiP layer cannot diffuse and is therefore constrained to stay at/below the TiP/InP interface. These pockets must therefore be composed of pure In whose peaks are observed on the corresponding diffractograms. One can notice that these pockets generate an important stress in the InP that might deteriorate the adhesion of the metallic layers on the substrate.

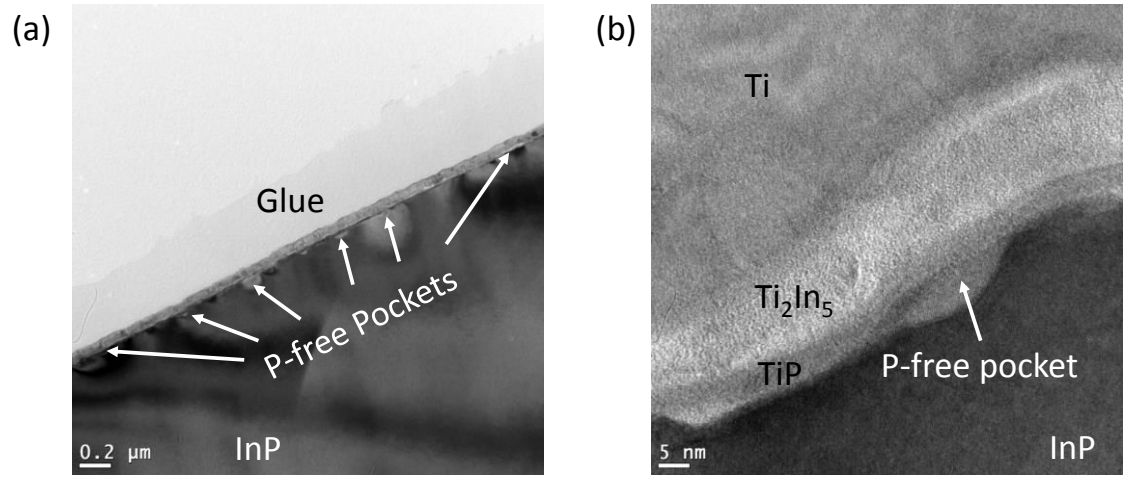


Figure 3.44: TEM cross section of the as deposited TiN(7 nm) / Ti (20 nm) / InP system showing the presence of P-free pockets below the TiP layer.

As a consequence, it appears that the Ti_2In_5 and the TiP are most probably formed simultaneously during the deposition process by reaction between the Ti and the InP surface submitted to the two steps surface preparation. Once the TiP layer is thick enough to be continuous, the reaction is inhibited and the system is stable up to 450 °C. At higher temperatures however, *i.e.* at 550 °C, a drastic change of composition is observed as the system is only composed of TiP and In. Therefore, during this annealing process, the Ti_2In_5 is decomposed into In which strongly diffracts and into additional Ti. This additional Ti along with the originally deposited one must meet the P contained in the substrate in order to enable the growth of the TiP. Therefore, a path must be created during this annealing process in order to allow the various species to move and meet. At this point, several hypotheses can be formulated.

(i) The increase in temperature might enhance the diffusion of the various compounds, therefore enabling them to diffuse fast enough through the TiP layer (Figure 3.45 (A)). This diffusion can occur in the bulk phase, via interstitial and/or substitutional sites or thanks to the grain boundaries. Depending on the diffusion coefficient associated to the Ti and P in this phase, the growth of this phase can occur at the Ti_2In_5/TiP interface, therefore limiting the length over which Ti would have to diffuse and/or at the TiP/InP interface, therefore limiting the length over which P would have to diffuse.

(ii) The second hypothesis that can be formulated lies on the assumption that the diffusion of the various species through the TiP layer is still too slow to enable any reaction. This layer must therefore become discontinuous / agglomerated at 550 °C in order to allow the Ti and P to interact[5] (Figure

[5] This situation would actually be similar to what was observed in the Ni/InP and Ni/InGaAs systems in which the intermetallic compounds are fully agglomerated at this temperature.

3.45 B). Note that the Ti_2In_5 layer might also be agglomerated as represented in Figure 3.45 B'. In both cases, once the Ti and the InP are in contact, the system tends to minimize its energy. As already mentioned, all the studies present in the literature report the formation of the TiP phase on intact InP surfaces, indicating the fact that this phase is the most stable on InP. As a consequence, because the few In-rich nanometers that were initially present on the InP have been consumed, the formation of the TiP phase is favored and associated to some In release to conserve the overall stoichiometry.

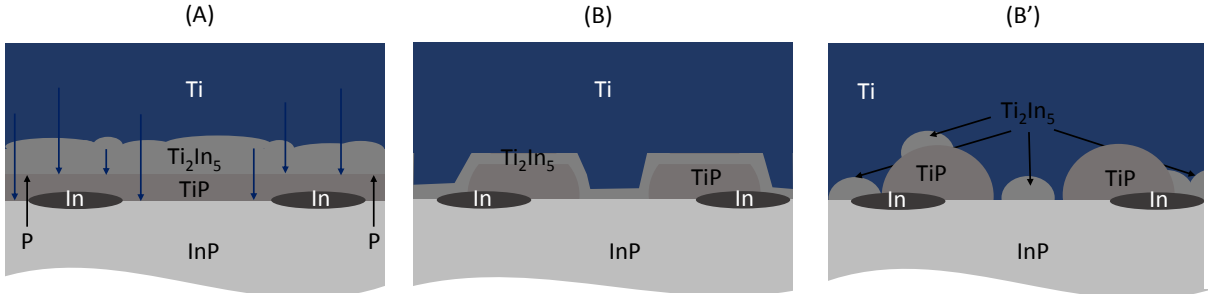


Figure 3.45: Schematic representation of the three situations that could enable the species to interact during the annealing treatment conducted at 550 °C. Note that these diagrams represent intermediate states occurring throughout the annealing process.

The second hypothesis appears to be the most likely firstly because the mechanisms related to the first one depend on the Ti thickness. The diffusion of the various species should indeed require much more time when 50 nm of Ti were deposited compared to the case were only 20 nm were initially present. Yet, the "Ti-20 nm" and "Ti-50 nm" seem to evolve similarly at 550 °C. Secondly, the electrical characterizations conducted on this system (see section 4.5.5) highlight a strong degradation of the electrical properties of this contact at 550 °C. The agglomeration of the layers at this temperature is therefore highly probable.

3.8.4 Summary of the results

In conclusion, we demonstrated that the reaction between Ti and the underlying InP substrate is initiated during the deposition process conducted at 100 °C. This reaction gives rise to the simultaneous formation of two binary phases, namely Ti_2In_5 and TiP. While the latter is largely reported in the literature, the first one had never been observed. We attribute the simultaneous formation of both phases to a compositional gradient induced in the InP by the wet surface preparation conducted in a concentrated HCl solution and enhanced by an in situ Ar^+ pre clean. In accordance with literature, the TiP layers is found to act as a diffusion barrier inhibiting further reaction up to 450 °C in spite of the presence of an important Ti reservoir. In this configuration, all

observed phases, *i.e.* Ti_2In_5, P, TiP and In, therefore coexist at temperatures up to 450 °C. Because the promotion of the TiP is thermodynamically more favorable, the Ti_2In_5 tends to be consumed in order to promote the TiP. However, this transition requires the appearance of a diffusion path within the TiP layer that is only be achieved at high temperature, *i.e.* at 550 °C. The growth of this phase is accompanied by an In release and a total consumption of the Ti_2In_5 and Ti. Therefore, at 550 °C the reaction is enabled either by the enhancement of the species diffusion through the TiP layer or by its agglomeration. This phase sequence along with the associated mechanisms is summarized in Figure 3.46.

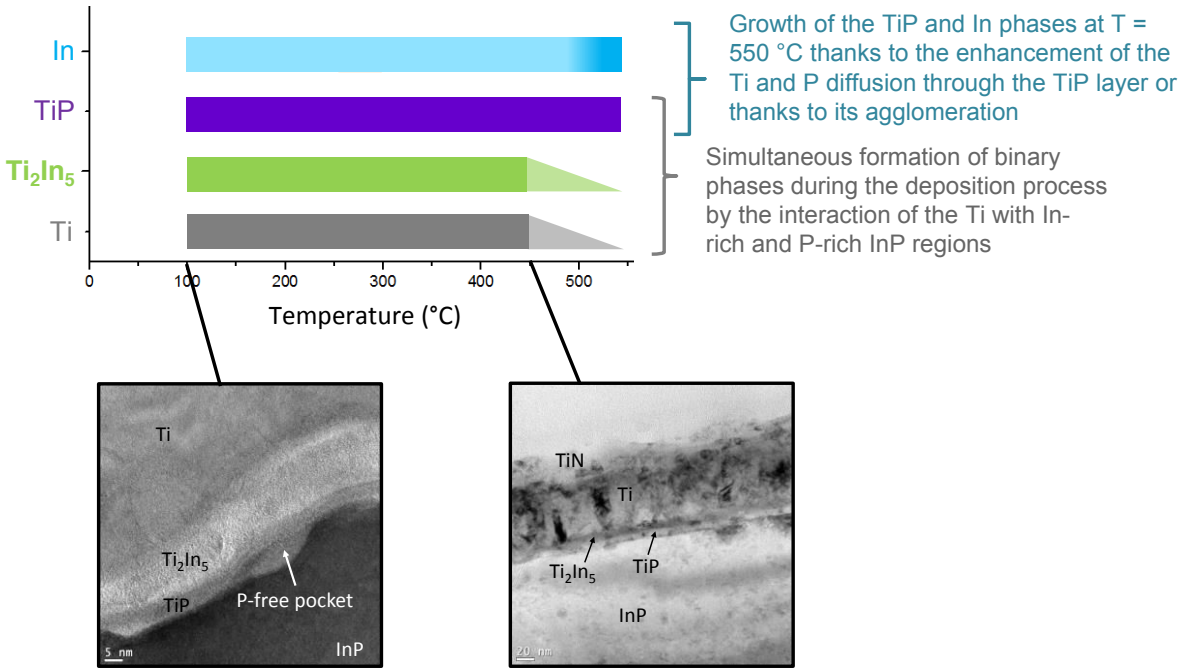


Figure 3.46: Summary of the metallurgical study conducted on the Ti/InP system. The light fillings correspond to temperatures that were not investigated and for which only trends on the phases' evolution are displayed.

3.9 Conclusion

This chapter was dedicated to the metallurgical study of Si-microelectronics compatible contacts to n-InP and p-InGaAs. Three different systems were morphologically and compositionally studied from deposition temperature to 550 °C.

First of all, the effect of the InP surface cleaning procedure including a dipping in a concentrated HCl solution (HCl : H_2O = 1 : 2) and an Ar^+ plasma pre-clean was studied. It appears that both processes result in the formation of a compositional gradient within the InP which is finally In-rich at its surface and P-rich underneath.

When a Ni layer is subsequently deposited by PVD, some Ni atoms interact with these modified regions to create a non-homogeneous α-Ni-In-P amorphous layer. After 60 s-RTP on Ni (20 nm) / InP, the phase sequence involves the coexistence of binary and ternary phases (Ni_2P, Ni_3P and $Ni_2(InP)$) which formation must be associated with some In partitioning in the early stages of the reaction. It is reasonable to assume that the Ar^+ plasma pre-clean plays an important role in this phase sequence as it results in P depletion of the substrate's surface. For short annealing durations (60 seconds) the binary Ni_2P phase grows at the expense of Ni_3P and $Ni_2(InP)$ as the annealing temperature increases and is coupled with an In precipitation or melting / solidification from 350 °C. At high temperature, *i.e.* at 550 °C, the layers are found to be fully agglomerated. Finally, it was found that the making of the binary and ternary compounds is controlled by the diffusion and/or by the interfacial reaction. On the contrary, the formation of In agglomerates from 350 °C is either linked to a melting/solidification process or to the precipitation of this compound controlled by the nucleation.

A similar study was conducted on p-InGaAs surfaces. It appears that the as deposited Ni/InGaAs is not modified by an annealing treatment conducted at 250 °C for 60 seconds. However, increasing the temperature up to 350 °C is sufficient to cause the total consumption of the Ni and the formation of a unique and uniform hexagonal phase which is $Ni_3(In_{0.53}Ga_{0.47})As$. The Ni was found to be the main diffusing species during the formation of this compound as highlighted by the conservation of the initial $In_{0.53}Ga_{0.47}As$ stoichiometry. On the contrary, at 550 °C, the Ni-containing compound is fully agglomerated and depleted in Ga and In. The phase formed at this temperature corresponds to a NiAs-like phase containing a small amount of In and Ga. In spite of this drastic change of stoichiometry, the crystallographic structure is not modified during the annealing treatments conducted at various temperatures.

Finally the investigation conducted on the Ti/InP system highlighted the initiation of a reaction between the Ti and the underlying InP during the deposition process conducted at 100 °C. The simultaneous formation of two binary phases, namely Ti_2In_5 and TiP, is attributed to the compositional gradient induced in the InP by the wet surface preparation and enhanced by the subsequent in situ Ar^+ pre clean. Once formed, the TiP layer acts as a diffusion barrier inhibiting further reaction up to 450 °C in spite of the presence of an important Ti reservoir. However, at higher temperature, the Ti_2In_5 tends to be consumed in order to promote the thermodynamically more favorable TiP. This transition requires the appearance of a diffusion path within the TiP layer that is only achieved at high temperature, *i.e.* at 550 °C. Therefore, at 550 °C the reaction is enabled either by the enhancement of the species diffusion through the TiP layer or by its agglomeration. The growth of this phase being accompanied by an In release and a total consumption of the Ti_2In_5 and Ti, the system is solely composed of TiP and In at 550 °C.

In the following chapter, the electrical properties of these systems will be probed. Thanks to the combined conclusions emanating from both chapters, we will be able to identify the most suitable metallization(s) for the formation of stable contacts with low specific contact resistivity on n-InP and p-InGaAs.

CHAPTER 3 - Bibliographic references

[1] P. Gas and F.M. d'Heurle. Formation of silicide thin films by solid state reaction. *Applied Surface Science*, 73(0):153 – 161, 1993.

[2] K. Maex and M. Van Rossum. *Properties of Metal Silicides*. INSPEC, the Institution of Electrical Engineers, 1995.

[3] S. P. Murarka. Silicide thin films and their applications in microelectronics. *Intermetallics*, 3(3):173 – 186, 1995.

[4] J.P. Gambino and E.G. Colgan. Silicides and ohmic contacts. *Mater. Chem. Phys.*, 52(2):99 – 146, 1998.

[5] F.M. d'Heurle. Silicide interfaces in silicon technology. *Journal of Electronic Materials*, 27(11):1138–1147, 1998.

[6] V. Borisenko. *Semiconducting Silicides*. Springer-Verlag Berlin Heidelberg, 2000.

[7] H. Iwai, T. Ohguro, and S-I. Ohmi. Nisi salicide technology for scaled CMOS. *Microelectronic Engineering*, 60:157–169, 2002.

[8] L. J. Chen. *Silicide Technology for Integrated Circuits*. The Institution of Electrical Engineers, 2004.

[9] M.B. Takeyama, A. Noya, T. Hashizume, and H. Hasegawa. Interfacial reaction and electrical properties in the sputter-deposited Al/Ti ohmic contact to n-InP. *Japanese Journal of Applied Physics*, 38(2S):1115, 1999.

[10] S.E. Mohney and Y.A. Chang. Phase formation in Ni/InP contacts. *Journal of Applied Physics*, 78(2):1342, 1995.

[11] X. Zhang, Ivana, H. X. Guo, X. Gong, Q. Zhou, and Y.-C. Yeo. A self-aligned Ni-InGaAs contact technology for InGaAs channel n-MOSFETs. *Journal of The Electrochemical Society*, 159(5):H511, 2012.

[12] P. Shekhter, S. Mehari, D. Ritter, and M. Eizenberg. Epitaxial NiInGaAs formed by solid state reaction on $In_{0.53}Ga_{0.47}As$: Structural and chemical study. *Journal of Vacuum Science & Technology B*, 31(3):031205, 2013.

[13] S. Mehari, A. Gavrilov, S. Cohen, P. Shekhter, M. Eizenberg, and D. Ritter. Measurement of the schottky barrier height between Ni-InGaAs alloy and $In_{0.53}Ga_{0.47}As$. *Applied Physics Letters*, 101(7):072103, 2012.

[14] L. Lu, H-D. Chang, B. Sun, H. Wang, B-Q. Xue, W. Zhao, and H-G. Liu. Solid phase reactions of Ni-GaAs alloys for high mobility III-V MOSFET applications. *Chinese Physics Letters*, 29(4):046802, 2012.

[15] L. Persson, M. El Bouanani, M. Hult, H. J. Whitlow, M. Andersson, I.F. Bubb, P.N. Johnston, S.R. Walker, D.D. Cohen, N. Dytlewski, C. Zaring, and M. Astling. Interfacial reaction studies of Cr, Ni, Ti, and Pt metallization on InP. *Journal of Applied Physics*, 80(6):3346–3354, 1996.

[16] N.S. Fatemi and V.G. Weizer. The structural and electrical properties of low-resistance Ni contacts to InP. *Journal of Applied Physics*, 73(1):289, 1993.

[17] T. Sands, C. C. Chang, A. S. Kaplan, V. G. Keramidas, K. M. Krishnan, and J. Washburn. Ni-InP reaction: Formation of amorphous and crystalline ternary phases. *Applied Physics Letters*, 50(19):1346, 1987.

[18] A. Yamaguchi, H. Asamizu, T. Okada, Y. Iguchi, T. Saitoh, Y. Koide, and M. Murakami. Near-noble transition-metal-based ohmic contacts to p-InP: Comparison of Ni and Pd as a base metal. *Journal of Applied Physics*, 85(11):7792–7796, 1999.

[19] V.G. Weizer, N.S. Fatemi, and A.L Korenyi-Both. Sinterless contacts to shallow junction InP solar cells. *Fourth International Conference on Indium Phosphide and Related Materials, 1992.*, pages 318–321, April 1992.

[20] A. Appelbaum, P. M. Thomas, and P. A. Barnes. Interaction of nickel with lnP as a fonction of annealing time and temperature. *Semiconductor - based heterostructures: Interfacila structure and stability*, page 409, 1986.

[21] D. G. Ivey, D. Wang, and P. Jian. Low temperature reactions between Nickel thin films and InP. *Experimental Methods of Phase Diagram Determination*, page 151, 1994.

[22] X. Zhang, H. Guo, X. Gong, Q. Zhou, Y.-R. Lin, H.-Y. Lin, C.-H. Ko, C. H. Wann, and Y.-C. Yeo. $In_{0.7}Ga_{0.3}As$ channel n-MOSFET with self-aligned Ni-InGaAs source and drain. *Electrochemical and Solid-State Letters*, 14(2):H60, 2011.

[23] X. Zhang, H. Guo, H-Y. Lin, Ivana, X. Gong, Q. Zhou, Y-R. Lin, C-H. Ko, C.H.. Wann, and Y-C. Yeo. Reduction of off-state leakage current in $In_{0.7}Ga_{0.3}As$ channel n-MOSFETs with self-aligned Ni-InGaAs contact metallization. *Electrochemical and Solid-State Letters*, 14(5):H212–H214, 2011.

[24] X. Zhang, H.-X. Guo, X. Gong, C. Guo, and Y.-C. Yeo. Multiple-gate $In_{0.53}Ga_{0.47}As$ channel n-MOSFETs with self-aligned Ni-InGaAs contacts. *ECS Transactions*, 45(4):P82–P85, 2012.

[25] Ivana, J. Pan, Z. Zhang, X. Zhang, H. Guo, X. Gong, and Y.-C. Yeo. Photoelectron spectroscopy study of band alignment at interface between Ni-InGaAs and $In_{0.53}Ga_{0.47}As$. *Applied Physics Letters*, 99(1):012105, 2011.

[26] L. Czornomaz, M. El Kazzi, M. Hopstaken, D. Caimi, P. Machler, C. Rossel, M. Bjoerk, C. Marchiori, H. Siegwart, and J. Fompeyrine. CMOS compatible self-aligned S/D regions for implant-free InGaAs MOSFETs. *Solid-State Electronics*, 74:71–76, August 2012.

[27] R. Chen and S.A. Dayeh. Size and orientation effects on the kinetics and structure of nickelide contacts to InGaAs fin structures. *Nano Letters*, 15(6):3770–3779, 2015.

[28] Ivana, Y. Lim Foo, X. Zhang, Q. Zhou, J. Pan, E. Kong, M. Samuel Owen, and Y.-C. Yeo. Crystal structure and epitaxial relationship of $Ni_4InGaAs_2$ *films formed on InGaAs by annealing*. *Journal of Vacuum Science* & *Technology B*: *Microelectronics and Nanometer Structures*, 31(1):012202, 2013.

[29] S. Zhiou, N.-T. Tra, Ph. Rodriguez, F. Nemouchi, Rapenne L., Blanc N., Boudet N., and P. Gergaud. Reaction of Ni film with $In_{0.53}Ga_{0.47}As$: Phase formation and texture. *Journal of Applied Physics*, 120:135304, 2016.

[30] S-L Zhang and F.M. d'Heurle. Modelization of the simultaneous growth of three intermediate phase. *Materials science forum*, 155/156:59–70, 1994.

[31] U.R. Evans. *The Corrosion and Oxidation of Metals: Scientific Principles and Practical Applications*. St. Martin's Press, 1960.

[32] B. E. Deal and A. S. Grove. General relationship for the thermal oxidation of silicon. *Journal of Applied Physics*, 36(12):3770–3778, 1965.

[33] F. Nemouchi, D. Mangelinck, C. Bergman, P. Gas, and Ulf Smith. Differential scanning calorimetry analysis of the linear parabolic growth of nanometric Ni silicide thin films on a si substrate. *Applied Physics Letters*, 86(4), 2005.

[34] D. Pramanik, A. N. Saxena, Owen K. Wu, G. G. Peterson, and M. Tanielian. Influence of the interfacial oxide on titanium silicide formation by rapid thermal annealing. *Journal of Vacuum Science & Technology B*, 2(4):775–780, 1984.

[35] W.J. Freitas and J.W. Swart. The influence of impurities on cobalt silicide formation. *Journal of The Electrochemical Society*, 138(10):3067–3070, 1991.

[36] C. Dehm, B. Raum, I. Kasko, and H. Ryssel. Influence of impurities on ion beam induced $TiSi_2$ formation. *Nuclear Instruments and Methods in Physics Research Section B: Beam Interactions with Materials and Atoms*, 80:759 – 763, 1993.

[37] A. E. Morgan, E. K. Broadbent, and D. K. Sadana. Reaction of titanium with silicon nitride under rapid thermal annealing. *Applied Physics Letters*, 49(19):1236–1238, 1986.

[38] M. F. C. Willemsen, A. E. T. Kuiper, A. H. Reader, R. Hokke, and J. C. Barbour. Insitu investigation of tin formation on top of $TiSi_2$. *Journal of Vacuum Science & Technology B*, 6(1):53–61, 1988.

[39] W.L. Bragg. The diffraction of short electromagnetic waves by a crystal. *Proceedings of the Cambridge Philosophical Society*, 17:43 to 57, 1913.

[40] B. D Cullity. *Elements Of X Ray Diffraction*. Addison-Wesley Publishing Company, Inc., 1956.

[41] B.E. Warren. *X-Ray Diffraction*. Dover Publications, 1990.

[42] C. Suryanarayana and M. Grant Norton. *X-Ray Diffraction: A Practical Approach*. Springer US, 1998.

[43] Y Waseda, E Matsubara, and K Shinoda. *X-Ray Diffraction Crystallography: Introduction, Examples and Solved Problems*. Springer-Verlag Berlin Heidelberg, 2011.

[44] A. Appelbaum, M. Robbins, and F. Schrey. Sputtered Ni-P as an ohmic contact to n-InP, p-InGaAs and as a diffusion barrier. *IEEE Trans. on Electron Devices*, ED-34(5), May 1987.

[45] T. Sands, V. G. Keramidas, K. M. Yu, J. Washburn, and K. Krishnan. A comparative study of phase stability and film morphology in thin-film M/GaAs systems (M=Co, Rh, Ir, Ni, Pd, and Pt). *Journal of Applied Physics*, 62(5):2070, 1987.

[46] S.E. Mohney and Y.A. Chang. Phase equilibria and ternary phase formation in the In-Ni-P system. *Journal of Materials Research*, 7(4):955–960, 01 1992.

[47] P.S. Mangat, P. Soukiassian, Y. Huttel, Z. Hurych, B. Gruzza, and A. Porte. Low energy Ar^+ ion bombardment induced modification of surface atomic bond lengths on InP(100) wafer. *Applied Physics Letters*, 63(14):1957–1959, Oct 1993.

[48] Q. Zhao, Z. W. Deng, R. W. M. Kwok, and W. M. Lau. Damage of InP (110) induced by low energy Ar^+ and He^+ bombardment. *Journal of Vacuum Science & Technology A*, 18(5):2271–2276, 2000.

[49] J-Y. Hu, W. Mahmood, and Q. Zhao. Effect of Ar^+, He^+, and S^+ irradiation on n-InP single crystal. *Chinese Journal of Chemical Physics*, 27(1):82–86, 2014.

[50] M. Ghaffour, A. Abdellaoui, M. Bouslama, A. Ouerdane, and B. Abidri. AES, EELS and TRIM simulation method study of InP(100) subjected to Ar^+, He^+ and H^+ ions bombardment. *EPJ Web of Conferences*, 29:00020, 2012.

[51] Ph. Rodriguez, L. Toselli, E. Ghegin, M. Rebaud, N. Rochat, N. Chevalier, E. Martinez, and F. Nemouchi. Cleaning of InGaAs and InP layers for Nanoelectronics and Photonics contact technology applications. *ECS Transactions*, 69(8):251–259, 2015.

[52] D. Cuypers, D. H. van Dorp, M. Tallarida, S. Brizzi, T. Conard, L. N. J. Rodriguez, M. Mees, S. Arnauts, D. Schmeisser, C. Adelmann, and S. De Gendt. Study of InP surfaces after wet chemical treatments. *ECS Journal of Solid State Science and Technology*, 3(1):N3016–N3022, 2014.

[53] Sujith Subramanian, Ivana, Qian Zhou, Xingui Zhang, Mahendran Balakrishnan, and Yee-Chia Yeo. Selective wet etching process for ni-InGaAs contact formation in InGaAs n-MOSFETs with self-aligned source and drain. *Journal of The Electrochemical Society*, 159(1):H16, 2012.

[54] S Zhiou. *Réaction à l'état solide d'un film mince de Ni(Co) avec InGaAs: analyses microstructurales*. PhD thesis, Université Grenoble Alpes, 2016.

[55] L. Zommer, A. Jablonski, L. Kotis, and M. Menyhard. Monte carlo calculation of backscattering factor for Ni-C multilayer system. *Journal of Physics D: Applied Physics*, 41(15):155312, 2008.

[56] A. Barna, S. Gurban, L. Kotis, J. Labar, A. Sulyok, A..L. Toth, M. Menyhard, J. Kovac, and P. Panjan. Growth of amorphous SiC film on Si by means of ion beam induced mixing. *Applied Surface Science*, 263:367 – 372, 2012.

[57] A. Barna, B. Kotis, L. Pecz, A. Sulyok, G. Safran, A.L. Toth, M. Menyhard, A. Kovacs, and A. Savenko. Thin TaC layer produced by ion mixing. *Surface and Coatings Technology*, 206:3917 – 3922, 2012.

[58] Ph. Rodriguez, L. Toselli, E. Ghegin, N. Chevalier, N. Rochat, E. Martinez, and F. Nemouchi. In situ cleaning of InGaAs surfaces prior to low contact resistance metallization. *Microelectronic Engineering*, 156:91 – 96, 2016.

[59] C. Perrin, E. Ghegin, S. Zhiou, F. Nemouchi, P. Rodriguez, P. Gergaud, P. Maugis, D. Mangelinck, and K. Hoummada. Formation of $Ni_3InGaAs$ phase in Ni/InGaAs contact at low temperature. *Applied Physics Letters*, 2019:131902, 2016.

[60] J.L. Labar. Consistent indexing of a (set of) single crystal SAED pattern(s) with the Process Diffraction program. *Ultramicroscopy*, 103:237–249, 2005.

[61] R. Guerin and A. Guivarch. Metallurgical study of Ni/GaAs contacts. I. Experimental determination of the solid portion of the Ni-Ga-As ternary-phase diagram. *Journal of Applied Physics*, 66(5):2122, 1989.

[62] A. Guivarch, R. Guerin, J. Caulet, A. Poudoulec, and J. Fontenille. Metallurgical study of Ni/GaAs contacts. II. Interfacial reactions of Ni thin films on (111) and (001) GaAs. *Journal of Applied Physics*, 66(5):2129, 1989.

[63] M.B. Takeyama, A. Noya, T. Hashizume, and H. Hasegawa. Study of chemical reactions at metal-InP interfaces formed by sputter deposition of Pt and Ti. pages 627–630. IEEE, 1998.

[64] D. Wang and D.G. Ivey. Interfacial reactions between Ti thin films and InP. *Materials Science and Engineering: B*, 41(2):289–293, November 1996.

[65] T. Kendelewicz, P. H. Mahowald, C. E. McCants, K. A. Bartness, I. Lindau, and W. E. Spicer. Chemical reaction and schottky barrier formation at the Ti/InP(110) and Sn/InP(110) interfaces: Reactive versus nonreactive cases. *Journal of Vacuum Science & Technology B*, 5(4):1033–1038, 1987.

[66] Th. Chasse, W. G. Wilke, and K. Horn. Chemical reactions and temperature-dependent interface formation of Ti/InP (110). *Surface and Interface Analysis*, 14(6-7):315–324, 1989.

[67] O. Yamazaki, K. Nakamura, H. Sakamoto, S. Ohnishi, and K. Sakiyama. In-situ rapid thermal nitridation of collimated titanium by physical vapor deposition as a blanket tungsten barrier. *Japanese Journal of Applied Physics*, 33(1S):466, 1994.

[68] G.D. Yao, Y.C. Lu, S. Prasad, W. Hata, F.S. Chen, and H. Zhang. Electrical and physical characterization of tin diffusion barrier for sub-micron contact structure. *MRS Proceedings*, 303, 02 2011.

CHAPTER 4

SI-COMPATIBLE OHMIC CONTACTS TO N-INP AND P-INGAAS: THEORY AND ELECTRICAL CHARACTERIZATION

Outline

In the previous chapters we presented an innovative contact integration scheme to III-V materials in the context of Silicon Photonics. Among other things, we explained the need to study new metallurgies that would form ohmic contacts on n-InP and p-InGaAs while being available in a front-end silicon microelectronics environment. To answer this need, two metals were selected: Ni and Ti. While one can choose to directly deposit the metal on the semiconductor, the silicidation process can also be transposed to III-V materials, therefore giving access to a wide range of phases. In this chapter we will theoretically present the electrical advantages of such an approach based on Metal / Semiconductor (abbreviated as M/SC) band diagrams. After that, we will present the electrical results obtained with Ni and Ti-based Si-compatible metallizations on n-InP and p-InGaAs. By linking the electrical results to the metallurgical ones presented in chapter 3, we will be able to propose the most suitable combination(s) for the formation of stable contacts lowering of the specific contact resistivity on n-InP and p-InGaAs. Finally, we will probe the impact of the various dielectric encapsulations that were presented in section 2.4 on the electrical performance of the contacts. Thanks to this overall study, we will be able to determine the most suitable dielectric encapsulation and metallizations on n-InP and p-InGaAs.

4.1 Metal / Semiconductor band diagrams and transport mechanisms

The specifications of the Silicon Photonics require the integration of contacts on the III-V laser with low specific contact resistivity (ρ_c). As presented in chapter 1, limit values of series resistance in the overall laser device are about 5 Ω, which induces a maximum of 0.5 to 1 Ω for each contact to minimize the Joule effect and the power consumption. The metallization(s) must therefore be selected to form ohmic contacts with specific contact resistivities lower than 5.10^{-5} Ω.cm². To fulfill this requirement, several technological solutions are available. In the following we will draw the M/SC band diagrams in order to theoretically explain how the conduction of such systems can be optimized [1-4].

4.1.1 Metal / Semiconductor band diagrams

The repartition of the charge carriers in metals and semi-conductors is commonly represented thanks to band diagrams. The latter depict the valence and conduction band-edge profiles derived from the alignment of the Fermi levels and are commonly used to predict the electrical behavior of M/SC contacts.

The theory of contacts between semiconductors and metals was developed by Mott and Schottky in 1938 [5, 6]. In the following we will deal with two M/SC contact limit cases. The first one is constituted by a metal and a semi-conductor, arbitrarily n-type, which does not present any interfacial states. The second case will be that of a contact presenting a non-zero density of surface states in the semiconductor, and a thin interfacial layer.

"Ideal contact" limit case

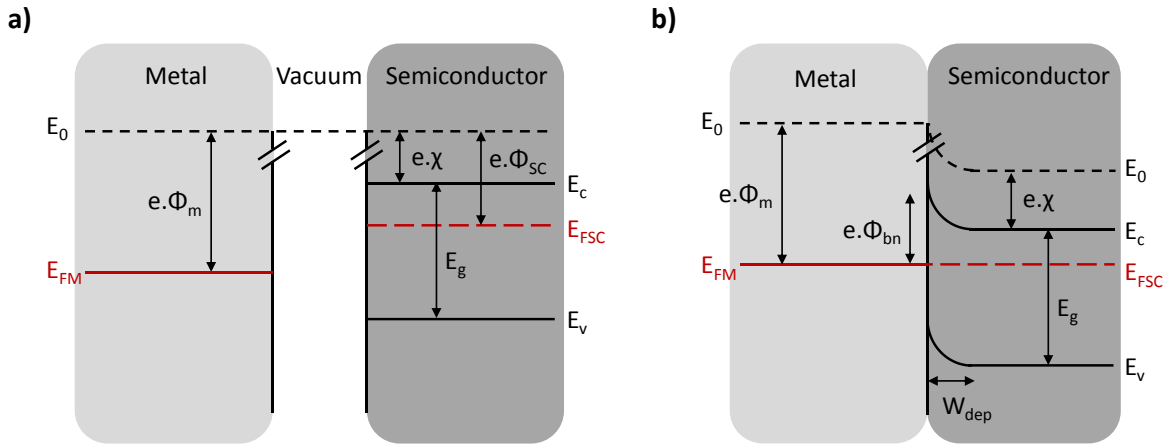


Figure 4.1: Simplified band diagrams of a M/n-SC system in the perfect limit case (a) before and (b) after contact.

Figure 4.1 depicts the band diagram of a M/SC system free from any interfacial states. Before contacting the metal and the semiconductor, the vacuum level E_0 is horizontal and the Fermi levels are distributed according to the work functions of each material, *i.e.*, Φ_M and Φ_{SC} (Figure 4.1(a)). The latter correspond to the energy required to remove an electron from the level of the chemical potential (E_F) and give it enough energy to escape to infinity, arriving there with zero energy. When the metal and semi-conductor are put in contact, electrons can lower their energy by flowing from the semiconductor to the metal, therefore generating energetic modifications in both materials Figure 4.1(b). In the semiconductor, the ionized donors N_D^+ are no longer compensated by the electrons which create a positively charged region in the semiconductor close to the interface called the *space charge region*. In the case depicted in Figure 4.1, it is more precisely a *depletion region* of width W_{dep}, where the bands are bent upwards. Similarly, a negatively charged region is created in the metal by the incoming electrons. This charge difference is responsible for the appearance of an electric field between the metal and the semiconductor. The equilibrium is reached when the diffusion of electrons from the semiconductor to the metal is compensated by the electric field-induced drift of electrons from the metal to the semiconductor. This equilibrium is characterized by a constant Fermi level throughout the structure ($E_{FM} = E_{FSC}$). The equilibrium Schottky barrier height (SBH) for electrons (Φ_{bn}) resulting from the band bending is exclusively determined by the metal work function (Φ_m) and by the semiconductor electron affinity (χ):

$$\phi_{bn} = \phi_m - \chi$$ **Equation 4.1**

A similar computation can be applied to p-doped semiconductors and the resulting Schottky barrier height is:

$$\phi_{bp} = E_g + e.\chi - e.\phi_m$$ **Equation 4.2**

Case of the contact with surface states

The reality is that the interfaces are never perfect and free of surface states. The latter are therefore always present and can be intrinsic or extrinsic [7, 8]. The intrinsic phenomenon, called Defect-Induced Gap States (DIGS), results from a crystalline lattice periodicity break close to the surface. While every atom situated in the volume is linked to all is neighbors, the bonds are only made on a half-plane close to the surface. Dangling bonds are thus generated, and the surface states are different from the volume ones. Therefore, the electronic wave functions that were considered as infinite in the bulk material are disturbed and states that were forbidden in the bulk gap are allowed in the surface's one. Quite similarly, extrinsic surface states can be generated by the presence of metallic adatoms on the surface of the semiconductor and are called MIGS (Metal Induced Gap State)[1]. In this case, the electronic wave function in the semiconductor must match that of an electron in the metal. Because the Fermi levels are aligned at thermal equilibrium, some states coming from the metal must decay into the semiconductor, allowing states in the gap at the interface. Finally, the presence of an interfacial layer such as a native oxide of thickness δ must be taken into account in most of the cases.

In the case of a system presenting surface states, the junction behavior is not ruled by the properties of the bulk materials but by those of the interface. This strong influence is due to the states that are present in the forbidden gap of the semiconductor. An energy level, Φ_0, corresponding to the position of the Fermi level for an electrically neutral surface is defined. The surface is electrically neutral if all the states situated below Φ_0 are filled with electrons while all the states situated above it are filled with holes. As a consequence, as soon as the Fermi level is not aligned with Φ_0, the surface is electrically charged. This results in the appearance of an electric field and therefore in a bending of the bands before contacting the metal with the semiconductor (ψ_{bi}). Figure 4.2 shows the band diagram of a metal semiconductor contact with a thin interfacial layer (δ), for *e.g.* a native oxide, and a large density of states. In this case, the semiconductor surface is already depleted in electrons before the realization of the contact (Figure 4.2(a)).

[1] Note that the MIGS are generated even in the presence of a thin interfacial layer between the metal and the semiconductor.

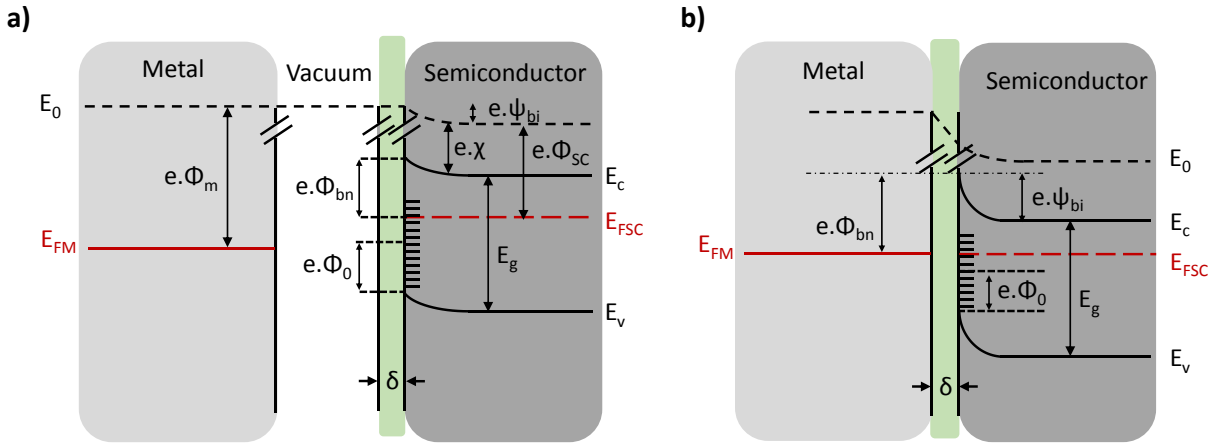


Figure 4.2: Simplified band diagrams of a M/n-SC system of a system with a thin interfacial layer and a non-zero density of states (a) before and (b) after contact.

Generally speaking, taking into account the presence of surface states, and respectively for n-doped and p-doped semiconductor, the Schottky barrier height can be written as [9]:

$$e.\phi_{bn} = \gamma(e\phi_m - e\chi) + (1-\gamma)(E_g - e\phi_0) \qquad \textbf{Equation 4.3}$$

$$e.\phi_{bp} = \gamma\left(E_g + e\chi - e\phi_m\right) + (1-\gamma)e\phi_0 \qquad \textbf{Equation 4.4}$$

The parameter $\gamma = \partial e\phi_b / \partial e\phi_m$ is specific to the considered metal / semiconductor couple and measures the sensibility of the Schottky barrier to the metal work function. If $\gamma = 1$, the metal work functions completely drives the Schottky barrier height; if $\gamma = 0$, the surface states are ruling the shape of the barrier and the Fermi level is said to be pinned. This parameter was shown to be strongly dependent on the type of bonds (covalent or ionic) of the semiconductor [2-4]. Its evolution is plotted as a function of the iconicity of the semiconductor, and more precisely as a function of electronegativity difference of the semiconductor constituents in Figure 4.3. One can notice that the InP and (In)GaAs compounds present an intermediate γ parameter which enables a barrier height tuning thanks to the nature of the metallic compound.

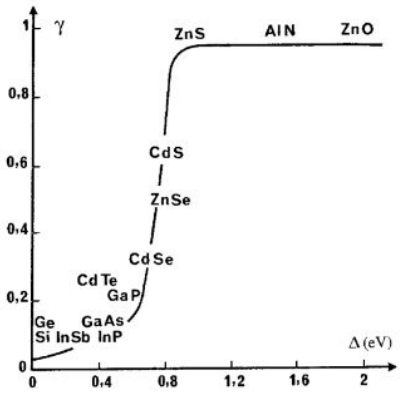


Figure 4.3: Variation of the parameter γ as a function of the electronegativity difference Δ of the semiconductor compounds.

The Schottky effect, or image force

When considering a practical contact, one must take into account an additional phenomenon: the Schottky effect, also known as the image force. The latter corresponds to a lowering of the barrier height caused by a force applied on the carriers in the presence of an electric field. More precisely, image charges build up in the metal electrode as carriers approach the metal-semiconductor interface. Indeed, when an electron is located at a distance *x* away from the metal, a positive charge of identical absolute value is generated at a distance –x with respect to the metal surface. The presence of two opposite charges with equal intensity creates an attraction which is called the image-force, given by:

$$F(x) = \frac{-e^2}{16.\pi.\varepsilon_0.x^2}$$ **Equation 4.5**

The work done by an electron during its path from infinity to the point x is given by:

$$\int_{\infty}^{x} F(x).dx = \frac{e^2}{16.\pi.\varepsilon_0.x^2}$$ **Equation 4.6**

This energy corresponds to the potential energy of the electron at a distance x from the metal surface. In presence of an electric field E, the resulting potential energy is given by:

$$E_p(x) = \frac{e^2}{16.\pi.\varepsilon_0.x^2} + e.E.x\ [J]$$ **Equation 4.7**

The Schottky barrier lowering (or image force lowering) $\Delta\Phi$ and its location along the x axis, x_m, are given by the condition $d\left[E_p(x)\right]/dx = 0$, and therefore:

$$x_m = \sqrt{\frac{e}{4.\pi.\varepsilon_0.E}}$$ **Equation 4.8**

$$\Delta\Phi = \sqrt{\frac{e.E}{4.\pi.\varepsilon_0}} = 2.E.x_m$$ **Equation 4.9**

The equations listed above are applicable to M/SC systems provided that the permittivity of free space is replaced by that of the semiconductor. The value of the electric field must also be replaced by that of the maximum electric field at the interface.

This barrier reduction is of interest since it depends on the applied voltage and leads to a voltage dependence of the reverse bias current. This Schottky lowering of the barrier is schematically represented in Figure 4.4.

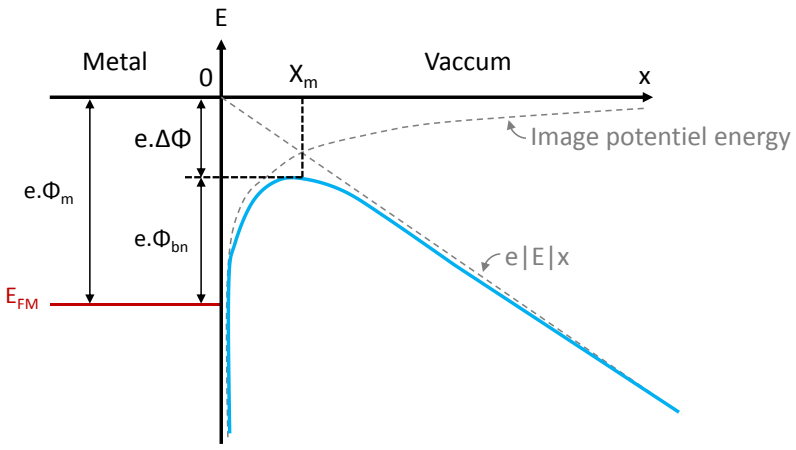


Figure 4.4: Energy band diagram between a metal surface and vacuum under an applied electric field E. The total potential energy of an electron in vacuum at a distance x from the metal surface is displayed taking into account the image force.

The resulting Schottky barrier height for electrons transiting from metal to n-doped and p-doped semiconductors is given by:

$$e.\phi_{bn} = \gamma(e\phi_m - e\chi - \Delta\Phi) + (1-\gamma)(E_g - e\phi_0)$$ **Equation 4.10**

$$e.\phi_{bp} = \gamma\left(E_g + e\chi - e\phi_m - \Delta\Phi\right) + (1-\gamma)e\phi_0$$ **Equation 4.11**

4.1.2 Current transport mechanisms

The presence of this barrier in M/SC systems results in the existence of various conduction modes that mainly rely on the majority carriers. These processes, listed below, will be qualitatively detailed

in the following section while the corresponding equations will be presented in Appendix A4. Note that both will arbitrarily deal with M/n-doped semiconductor systems.

1. The thermionic emission (TE) corresponds to the transport of electrons from the semiconductor to the metal, and vice versa, above the barrier;
2. The diffusion of electron corresponds to a displacement of the charge carriers from the bulk semiconductor to the space charge region;
3. The field emission (FE and TFE) corresponds to the tunneling of the electrons through the barrier;
4. Electron / hole pairs can be recombined in the space charge region;
5. The electron / hole pairs can also be recombined in the neutral region, which corresponds to a diffusion of the holes from the metal in the semiconductor (hole injection).

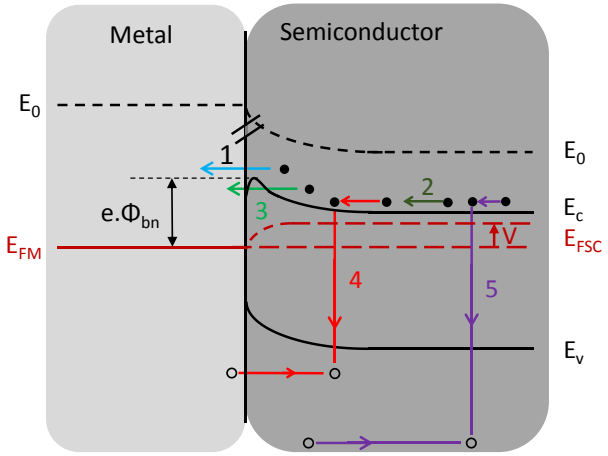


Figure 4.5: Schematic representation of the five current transport mechanisms across a M/n-SC junction under forward bias. Note that the bias is applied on the semiconductor, the reference being the position of the metal Fermi level derived from the metal work function, Φ_m.

Emission over the barrier

The transit of electrons above the Schottky barrier can be realized thanks to two different mechanisms, which are actually the two limit cases of this phenomenon. In the case of high mobility semiconductors, the transport can be described by the thermionic emission (TE) while the dominant mechanism for low mobility semiconductors is the diffusion. Practically these two phenomena are combined and the true conduction behavior lies somewhere in between these extrema.

The diffusion theory was firstly proposed by Schottky in 1938 [5]. Generally speaking, the current fluxes result from the displacement of charge carriers under a force. In the case of the drift / diffusion theory, the latter can be due to the presence of an electric field E(x) (drift) and/or from a

concentration gradient (diffusion). Whatever the driving force, the drift-diffusion rules the way the charge carriers manage to reach the interface.

The thermionic emission (TE) corresponds to the transit of the charge carriers from the semiconductor to the metal above the barrier and was firstly theorized by Bethe [2, 10, 11]. In this case, the shape of the barrier is unimportant as the current flux only depends on its height. Therefore, if the thermal energy is important enough, it enables the transit of electrons above the barrier. When the thermal equilibrium is reached, the electron flux from the semiconductor to the metal exactly compensates that from the metal to the semiconductor. The resulting current density (J) across the barrier is equal to zero. The forward polarization ($V_F > 0$) of the contact results in an upward shift of the semiconductor's Fermi level of magnitude $e.V_F$. As a result, the barrier height seen by the electrons flowing from the semiconductor to the metal is lowered by the same quantity and the current density in forward direction (SC → M) is larger than it is in reverse direction (M → SC). A reverse polarization ($V_R < 0$) lowers the semiconductor Fermi level which results in a displacement of the charge carriers from metal to semiconductor. These situations are schematically represented in Figure 4.6.

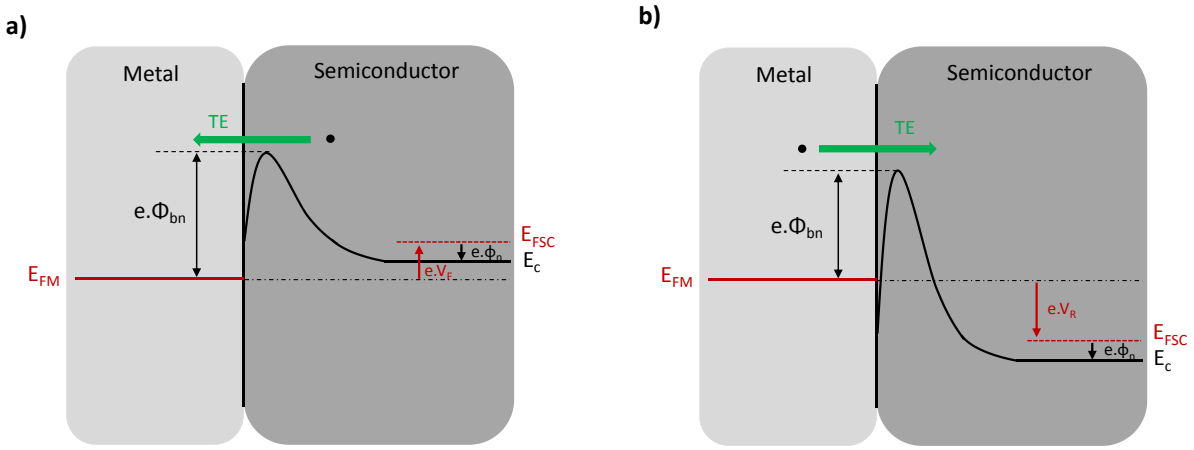


Figure 4.6: Illustration of the TE conduction mode in a M/n-SC contact under (a) forward bias and (b) reverse bias.

General description of the FE and TFE conduction modes

In the previous paragraphs we presented the conduction modes in which the charge carriers go from one side of the barrier to the other by getting over it. This kind of approximation is well adapted for moderately doped semiconductors in forward bias where the TE mode is dominant. However, in many cases, and especially under reverse bias, a non-negligible part of the charge carriers tunnel through the barrier. This process allows the electrons that have energy lower than that of the barrier top to cross it. Two main situations can arise in that case under forward and reverse bias, and are schematically represented in Figure 4.7.

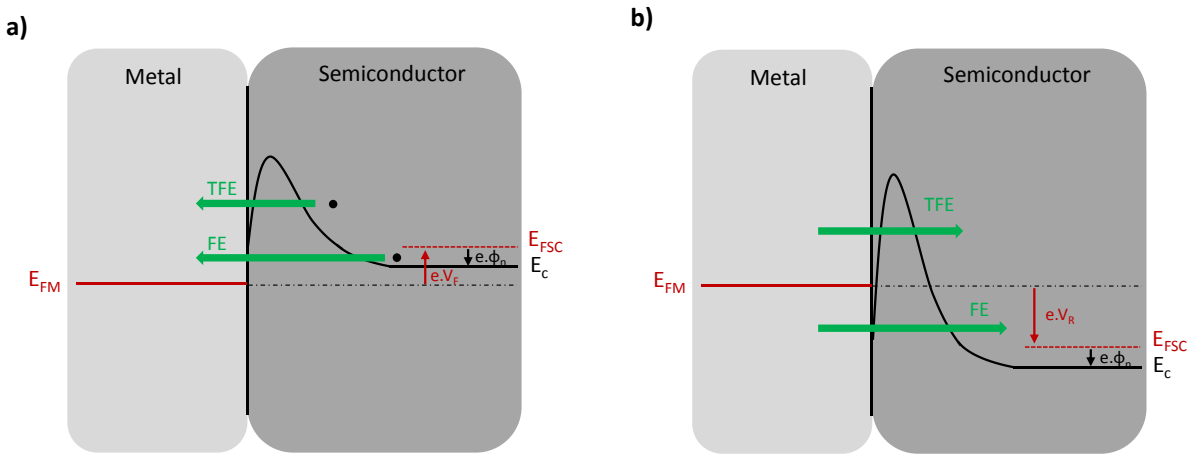


Figure 4.7: Illustration of the FE and TFE conduction modes in a M/n-SC contact under (a) forward bias and (b) reverse bias

In highly doped semiconductors, *i.e.* in degenerate semiconductors, and in forward polarization, the current mainly results from the tunneling of electrons with energies lower than the Fermi level of the semiconductor. This process corresponds to the field emission (FE) as described in Figure 4.7. The ohmic characteristic of I(V) curves (linear dependence of I as a function of V) of contacts to heavily doped semiconductors often results from an important tunneling across a Schottky barrier. When increasing the temperature, some electrons are promoted in higher energy levels. Because of the quasi-triangular shape of the barrier, the probability of tunneling increases for these charge carriers as the barrier gets thinner. This phenomenon, called thermionic field emission (TFE) is schematically represented in Figure 4.7. If the temperature is further raised, some charge carriers might even reach an energy high enough to go over the barrier (TE).

4.2 From Metal / Semiconductor band diagram to the specific contact resistivity

4.2.1 Definition of the contact resistance and resistivity

As explained in the previous sections, the transport of current from metal to semiconductor (and vice versa) relies on, and is limited by various transport mechanisms both in the presence of positive and negative Schottky barrier. In the latter case, the various conduction modes enabling the charge carriers to go through or above the barrier, *i.e.* FE, TFE and TE, depend on the applied voltage. As a consequence, in the general case the resulting density of current might depend on the applied bias,

therefore giving rise to non-linear I(V) characteristics. In order to account for all possible cases, the general definition of the contact resistivity is:

$$\rho_C\ [ohm.cm^2] = \left(\frac{\partial J}{\partial V}\right)^{-1}_{V=0}$$ **Equation 4.12**

With J the current density and V the polarization of the contact.

Taking into account the dimensions of the contact, the value of the contact resistance can be derived as:

$$R_C = \frac{\rho_C}{A}\ [Ohm]$$ **Equation 4.13**

Where A is the area through which the charge carriers cross the M/SC interface.

4.2.2 Metal / Semiconductor system presenting a negative barrier

To lower the contact resistivity, the formation M/SC systems presenting negative Schottky barriers would be the most efficient solution. In this case, the charge carriers would flow from metal to semiconductor, and vice versa, in the same way. This situation is schematically represented on n- and p-type semiconductors in Figure 4.8.

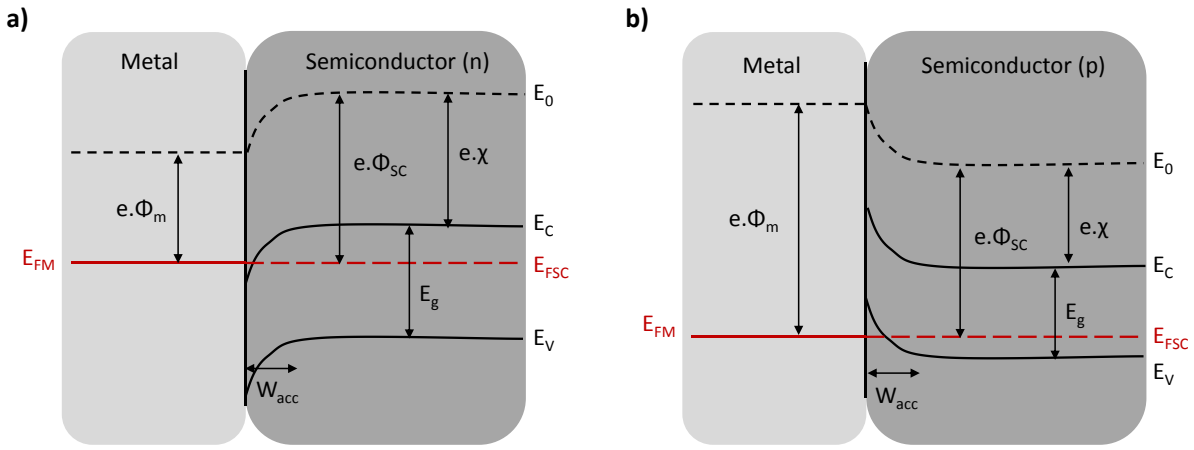


Figure 4.8: Illustration of ohmic contacts (a) to an n-doped semiconductor (b) to a p-doped semiconductor at V=0 .

Under the assumption that the Fermi level is not pinned, the formation of such contacts requires the use of metals such as:

- For n-type semiconductors: $\phi_M < \phi_{SC}$
- For p-type semiconductors: $\phi_M > \phi_{SC}$

This simple consideration highlights the fact that the formation of negative barriers on p-InGaAs ($\phi_{p-InGaAs} = 5.29\ eV$) would require the use of metals with high work functions. Among the common metals, only the Pt presents a suitable work function ($\phi_{Pt} = 5.3\ eV$) but the difference is poor and might not result in good electrical characteristics. In any cases, the realization of Pt-based contacts would also be too expensive to be industrialized.

The ideal case of negative barrier is thus strongly compromised by the limited amount of suitable metals, especially on p-doped semiconductors. Therefore, in most M/SC systems, a positive Schottky barrier is present at the interface. However, we highlighted in section 4.1.2 that while this barrier slows down the conduction it does not necessarily cease it. In the following we will present the available levers to enhance the conduction modes in the presence of a Schottky barrier.

4.2.3 Enhancement of the conduction above and through the barrier

These conduction modes, namely TE, FE and TFE, are schematically represented in Figure 4.9 arbitrarily for M / n-type SC systems.

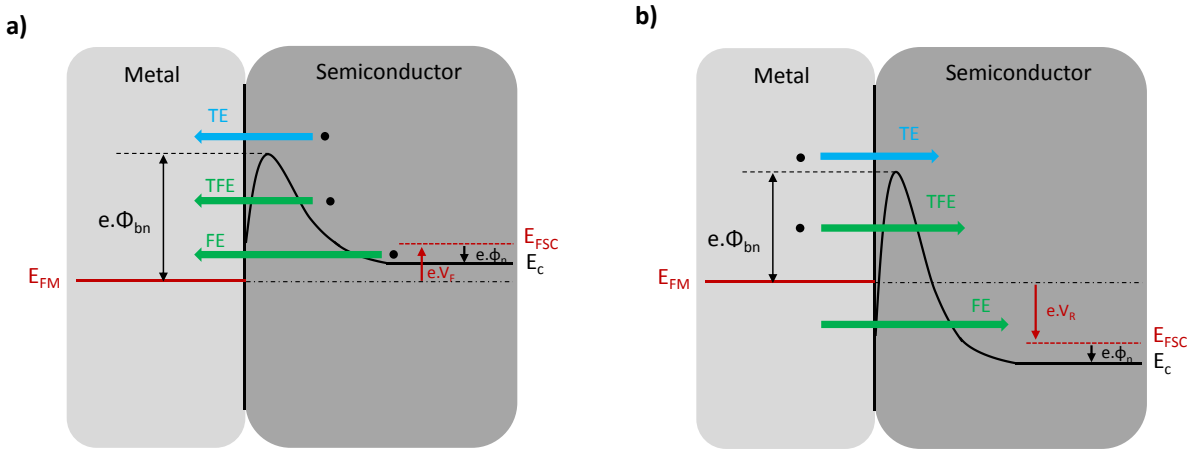


Figure 4.9: Schematic representation of the TE, FE and TFE conduction modes in a M/n-SC system (a) under forward bias and (b) under reverse bias.

Enhancement of the field effect

The improvement of the conduction through a Schottky barrier can firstly be achieved by favoring the tunneling processes, *i.e.* the FE and TFE modes. Increasing the tunneling probability requires a thinning of the barrier, *i.e.* of the space charge region whose width is inversely proportional to the

doping level of the semiconductor[2]. As a consequence, the semiconductors' doping levels are generally high in M/SC systems, and reach, in our case, $N_D = 5.10^{18}$ cm^{-3} in n-InP and $N_A = 3.10^{19}$ cm^{-3} p-InGaAs. Directly doping the epitaxy offers a double advantage as it also allows decreasing the semiconductor sheet resistance (R_{SH}) were electrons and holes flow before reaching the contact region. On top of that the additional use of localized doping techniques is of great interest because:

- The width of the depletion layer is mainly affected by the doping level of the semiconductor surface;
- The bulk doping levels remain limited by the solubility limit of the doping species;
- A high concentration of ionized atoms underneath the active region of the laser would generate optical losses.

As a consequence, the semiconductor epitaxies are generally doped during their growth and localized dopings can be performed afterwards. For example, in the case of the laser where the n-InP and p-InGaAs epitaxies are respectively doped at $N_D = 5.10^{18}$ cm^{-3} and $N_A = 3.10^{19}$ cm^{-3}, one could imagine to realize an ion implantation after the contact cavities opening [12-14]. However, this solution firstly amorphizes the semiconductor surface and requires the use of a thermal treatment to recover the crystallinity. The latter is often performed at high temperature (T > 600 °C) which could compromise its use on a laser. A more gentle solution, the gas immersion laser doping (GILD), was also developed on Si surfaces where it allows reaching doping concentrations above the solubility limit [15-17].

Lowering of the Schottky barrier height

Secondly, one must consider the TE conduction mode whose amplitude depends on the Schottky barrier height Φ_{bn} or Φ_{bp} (cf Equation 4.10 and Equation 4.11). The latter can be tuned by changing the metal in contact with the semiconductor provided that the Fermi level is not pinned by the surface states. As presented in section 4.1.1 and more precisely in Figure 4.3, it is the case for InP and InGaAs where surface states play an important role but where the Fermi level is not completely pinned. Therefore, on these semiconductors, the metallic compound in contact with the semiconductor modifies the resulting Schottky barrier height.

One can thus choose to deposit an appropriate metal on the semiconductor surface. However, this solution can be delicate as:

- The quantity of available metals is limited;

[2] Because of the quasi-triangular shape of the Schottky barrier, lowering its height is also beneficial for the enhancement of the FE and TFE modes. The solutions available to lower this maximum energy are presented in the next section entitled "Lowering of the Schottky barrier height".

- The semiconductor's surface condition is of crucial importance. For example, it must not be deteriorated by the surface preparation or the metal deposition process and must not present any oxide or contaminant;
- The thermal stability of the deposited phase(s) might be poor and the resulting system might be altered by the thermal budgets applied during the overall integration of the device.

To overcome the last restriction, one can choose to deposit the phase(s) of interest and to stabilize it (them) thanks to an annealing process. However, this solution does not lower the impact of the semiconductor surface condition on the resulting resistance and gives access to a limited range of compounds. To overcome these restrictions, one can choose to form intermetallic compounds by solid state reaction with the semiconductor. Tuning the deposited metal, the annealing temperature and duration leads to a significant variation of the phases' nature. This kind of process therefore gives access to a wider range of metal work functions and then to a potential lowering of the Schottky barrier height. Moreover, the formation of intermetallic compounds often consumes contaminants and defects at the original metal/semiconductor interface, therefore limiting their impact. Although it has not been proved, we assume that this process might as well reduce the DIGS by creating a graduate transition from metal to semiconductor.

Consequently, coupling the thinning of the Schottky barrier by means of a high doping with its height lowering thanks to the adaptation of the metal work function are key to enhance the TE, FE and TFE conduction modes, and therefore to lower the specific contact resistivity.

4.2.4 Resulting I(V) characteristics

Enhancing the conduction modes in a M/SC system allows the charge carriers to flow in a similar way from metal to semiconductor and the other way around over a certain range of applied voltage around 0 V. Therefore, over this range of voltage, the resistance that they encounter does not depend on the applied voltage and the resulting I(V) curve respects the Ohm's law, *i.e.* is linear.

On the contrary, in a Schottky contact the conduction from metal to semiconductor (reverse current) and from semiconductor to metal (forward current) are very different from one another. The resulting I(V) curve is that of a diode and is therefore asymmetrical. Both configurations are schematically represented in Figure 4.10.

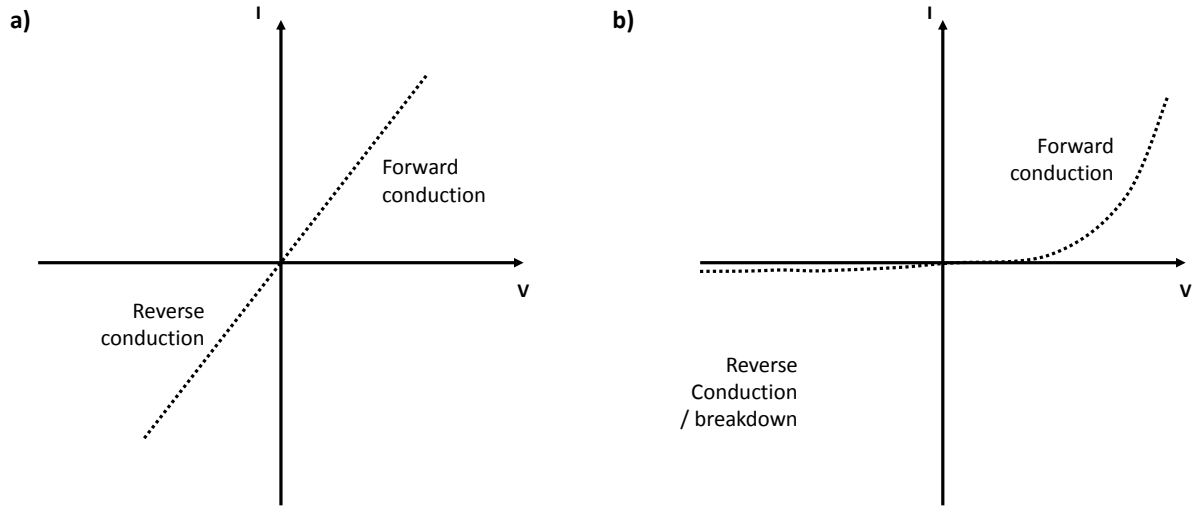


Figure 4.10: Schematic representation of the I(V) curves in the case of (a) a ohmic contact and (b) a Schottky contact

4.3 The Transfer Length Method (TLM)

4.3.1 Measurement principle

The contact resistance, R_C, and resistivity, ρ_C, being key parameters to evaluate the electrical performances of contacts, various experimental setups and methods allowing their extraction are available. One of the most common relies on the use of the Transmission Line Model and on the Transfer Length Method (both abbreviated as TLM)[3]. The latter were independently proposed by Berger *et al* and Murrmann *et al* in 1969 [18, 19]. Although these theories give a first qualitative insight, they were largely discussed over the years [20, 21]. The specific contact resistivity was indeed extracted by subtracting two large quantities, therefore leading to a non-negligible uncertainty. The TLM experiment was thus refined over the years including additional inputs from Shockley *et al* [22-25]. The resulting data extraction enables a decorrelation of the actual contact's contribution from that of the underlying semiconductor thanks to an array of identical contacts separated by an increasing distance (Figure 4.11).

[3] The transmission line model applied to the case of M/SC contacts comprises the current and voltage equations describing the conduction in such systems. The Transfert Length Method capitalizes this model in order to extract contact resistances and resistivities thanks to a three-terminal resistor structure.

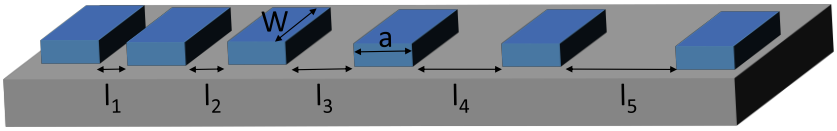


Figure 4.11: Schematic representation of a TLM structure. All contacts are identical (width *W* and length *a*, and separated by an increasing distance l_i.

Thanks to a four probe measurements, the I(V) curves corresponding to each couple of adjacent contacts are acquired. The probed voltage range is chosen to cover the operating point of the targeted device. At this point, a first stage of selection must be realized:

- If the contacts are Schottky, the I(V) curves are not linear. The resistance varies with the applied voltage and a quantitative extraction of the contact resistance R_C is thus impossible.
- If the contacts are ohmic, the I(V) curves are linear. In this case, the inverse of the slope gives access to the resistance R_{tot}.

It is important to note that the measured resistance (R_{tot}) results from the contribution of not only the probed contacts (R_C), but also of the underlying substrate (R_{sub}) as represented in Figure 4.12. The metallic pads presenting a sheet resistance at least two orders of magnitude lower than that of the semiconductor, they will be considered as constant potential planes in the following.

$$R_{tot} = 2.R_C + R_{SH}.\frac{l_i}{W}$$ **Equation 4.14**

With R_{SH} the sheet resistance of the underlying semiconductor.

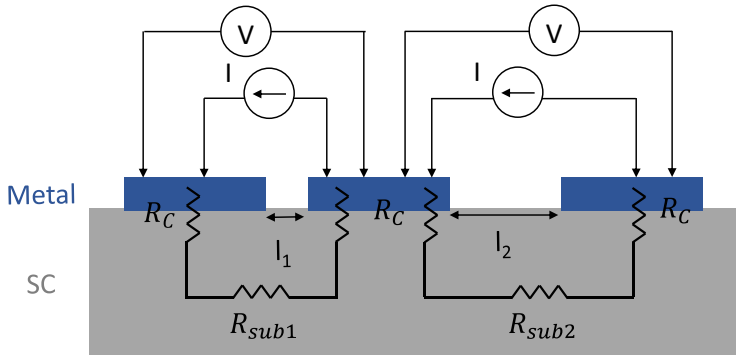


Figure 4.12: Schematic representation of the resistances contributing to the overall measured resistance in a TLM. Note that the contacts are considered as ohmic in this diagram.

The resistance corresponding to the substrate (R_{sub}) is always constant and might cover up the variations of the contact resistance with the applied voltage in the case of a Schottky contact. Therefore, in order to maximize the contribution of the contacts with respect to that of the substrate, the first selection step must be realized on small spacings, *i.e.* on spacings lowering the

substrate's contribution compared to that of the contacts. If the corresponding I(V) curve is linear, the contacts are most likely ohmic and a quantitative extraction of the specific contact resistivity can be conducted[4].

4.3.2 Important definitions

The quantitative extraction of the specific contact resistivity thanks to the TLM requires the definition of key parameters that we will detail in the following section.

Current crowding

The current flowing from one metallic pad to the other might deviate from a linear trajectory. This effect is called the crowding effect and leads to important measurement errors. To force the current lines to stay linear and parallel to one another, the semiconductor is patterned close to the metallic pads edges as represented in Figure 4.13. This etching corresponds to the definition of the so called mesa. The confinement of the charge carriers in the vertical direction is achieved by thinning the semiconductor layer. However, the final thickness must not be too thin to limit the parasitic resistance linked to the constriction effect.

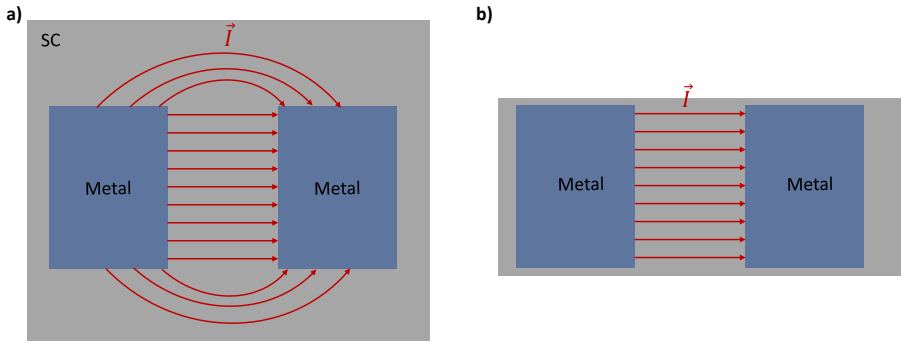


Figure 4.13: Illustration of (a) the crowding effect and (b) the current lines in the case of a patterned structure.

Transfer length, L_T

When flowing from one metallic pad to another, the charge carriers have to cross the first M/SC interface, travel through the doped semiconductor before crossing the second SC/M interface. The position where the current actually crosses the M/SC interfaces results from a competition between the contact resistivity (ρ_C) and the semiconductor's sheet resistance underneath the contact region

[4] Unfortunately, when acquiring I(V) characteristics thanks to the TLM method, one must be aware that the substrate's contribution might participate to the linearity of the curve. Lowering the spacing is necessary to limit this contribution but does not suppress it. In order to optimize this data treatment, cross bridge kelvin resistors were integrated on the layout of the second mask that was developed (TASP) and will enable an accurate determination of the contacts' I(V) characteristics.

(R_{SH} or R_{SK}, see below). This phenomenon is represented by the transfer length, noted L_T as represented in Figure 4.14 and defined in Equation 4.13.

$$L_T = \sqrt{\frac{\rho_C}{R_{SK}}}$$ **Equation 4.15**

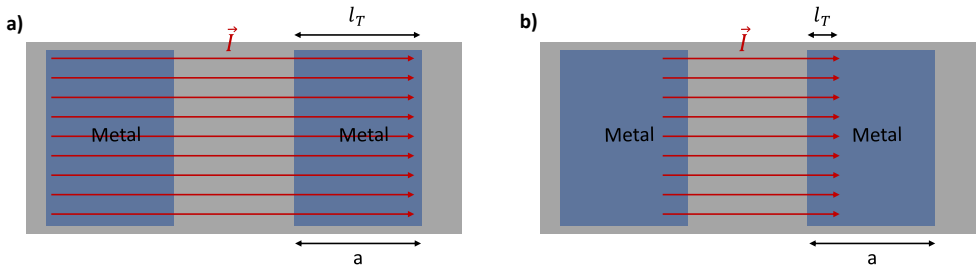


Figure 4.14: Illustration of the transfer length in the case where (a) $L_T \sim a$ and (b) $L_T \ll a$.

Sheet resistance of the semiconductor

Another important parameter to consider is the sheet resistance of the semiconductor. Indeed, while it might be constant throughout the path of the charge carriers (R_{SH}), applied thermal budgets might also modify it locally underneath the contacts (R_{SK}). This can for example result from segregation or accumulation (snow plow) of the doping species below the intermetallic compound(s) [26-28]. This situation, schematically represented in Figure 4.15, directly impacts the value of the transfer length L_T.

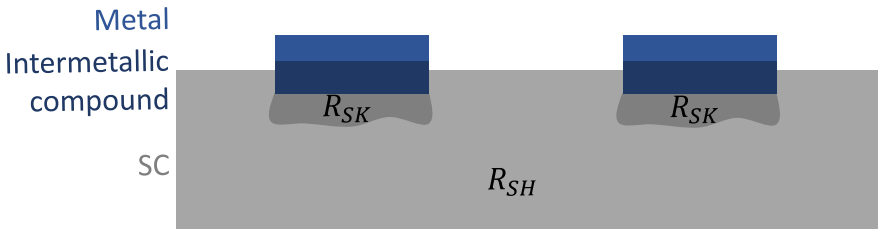


Figure 4.15: Schematic representation of the modification of the semiconductor's sheet resistance underneath the contact.

4.3.3 Extraction of the specific contact resistivity – general case

The general terms being defined, the specific contact resistivities can be extracted on contacts featuring an ohmic behavior [24, 25]. To do so, the resistances corresponding to all spacings are extracted and plotted as a function of the latter. The resulting plot should feature a linear trend as represented in Figure 4.16.

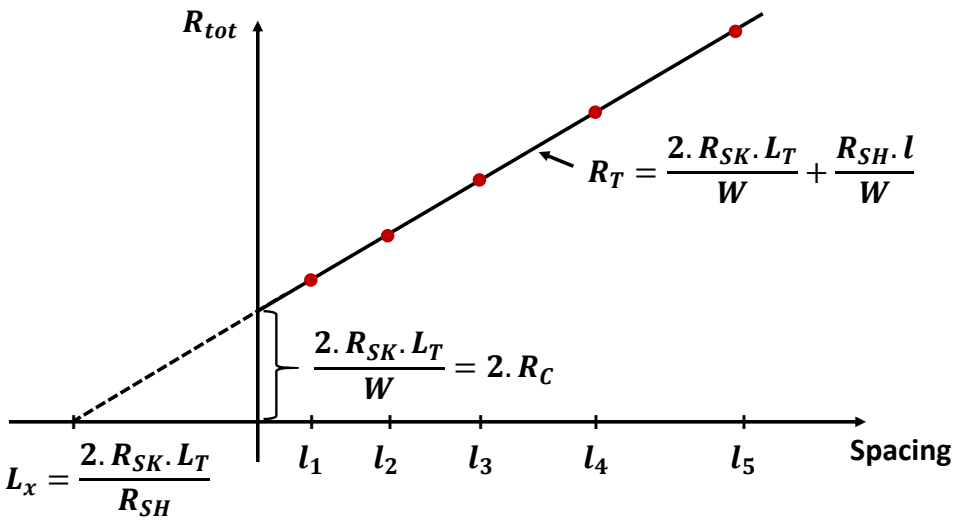


Figure 4.16: Schematic representation of the $R_{tot}(l_i)$ plot used to extract the specific contact resistivity in the case of a TLM experiment.

Thanks to it, the various parameters electrically characterizing the contact can be extracted. First of all, the sheet resistance of the bulk semiconductor R_{SH} can be directly derived from the slope of the curve.

$$R_{SH} = slope\ .W \qquad \textbf{Equation 4.16}$$

In the case of a non-alloyed contact, R_{SH} and R_{SK} are identical. The extrapolation of the curve to $y = 0$, noted L_x, therefore gives access to the transfer length L_T.

$$L_T = {}^{L_x}/_{2} \qquad \textbf{Equation 4.17}$$

Finally, the intercept of the curve represents the case where the substrate's contribution is suppressed. As a consequence, the corresponding resistance is twice the contact resistance.

$$Intercept = 2.R_C \qquad \textbf{Equation 4.18}$$

The specific contact resistivity can be directly extracted from these parameters:

$$\rho_C = R_C.A \qquad \textbf{Equation 4.19}$$

where A is the contact area crossed by the charge carriers. Taking into account the transfer length defined in the previous section, Equation 4.19 becomes:

$$\rho_C = R_C.L_T.W \qquad \textbf{Equation 4.20}$$

An additional correction directly derived from the transmission line model is applied (the reader interested in the overall computation can refer to Appendix A5). The latter allows taking into account

the current crowding that can occur between the two probed contacts. The resulting and final expression of the contact resistance and specific contact resistivity is:

$$R_c = \frac{R_{SK}.L_T}{W}.cth(\frac{a}{L_T}) \quad \textbf{Equation 4.21}$$

$$\rho_C = \frac{R_C.L_T.W}{cth(a/L_T)} \quad \textbf{Equation 4.22}$$

4.3.4 Extraction of the specific contact resistivity – alloyed contacts

In the case of alloyed contacts, the extraction of the specific contact resistivity is very similar. However, because R_{SH} and R_{SK} might differ, the computation of the transfer length requires additional steps [24, 25, 29-31]. For this purpose, the end resistance, noted R_E and corresponding to the drop of voltage occurring at the end of the contacts was introduced [23][5]. The latter is defined as:

$$R_E = \left.\frac{v_2}{i_1}\right|_{i_2=0} \quad \textbf{Equation 4.23}$$

Where v_2 corresponds to the drop of voltage between the contacts C_2 and C_3 when a current i_1 is injected between the contacts C_1 and C_2 (Figure 4.17). Because of the infinite input impedance of the voltmeter, this drop of voltage theoretically occurs solely in the second contact, and therefore corresponds to R_{C2}, *i.e.* to R_E.

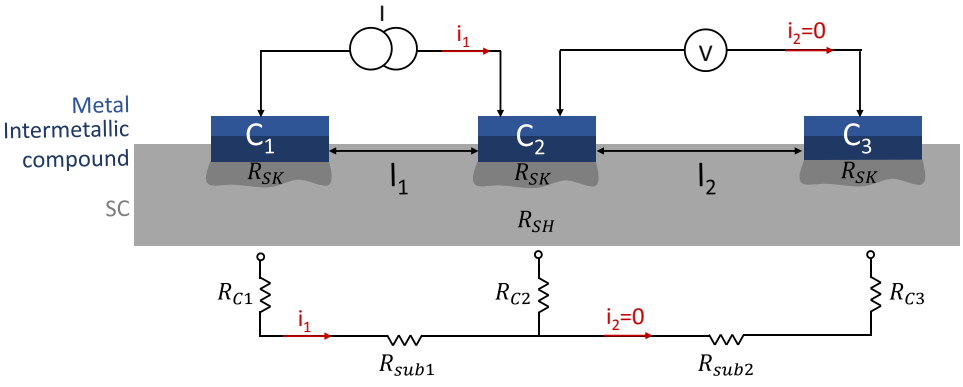


Figure 4.17: Experimental setup used for the determination of the end resistance (Setup A).

Based on Equation 4.23 and on the Transfer Length Method detailed in appendix A5, one can express the end resistance as:

[5] Oddly enough, the notion of end resistance was originally introduced by Shockley *et al* [23] to address the electrically short contacts ($d < L_T$) with no reference to the alloyed contacts.

$$R_E = \frac{R_{SK}.L_T}{W}.\frac{1}{\sinh(a/L_T)}$$ **Equation 4.24**

Finally, the ratio between R_C (Equation 4.21) and R_E (Equation 4.24) allows a determination of the transfer length:

$$\frac{R_C}{R_E} = \cosh(\frac{a}{L_T})$$ **Equation 4.25**

The specific contact resistivity can therefore be calculated based on Equation 4.22.

Another experimental setup was proposed to determine the value of the end resistance as schematically represented in Figure 4.18.

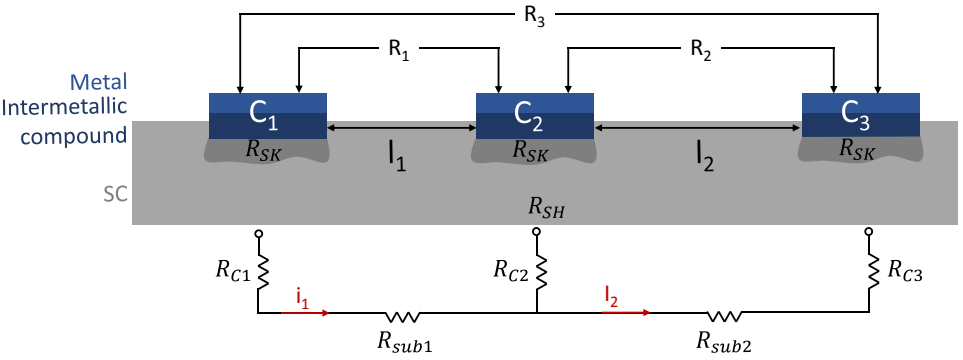


Figure 4.18: Experimental setup used for the determination of the end resistance (Setup B).

The extraction of R_E thanks to this setup is achieved by measuring the resistances R_1 , R_2 and R_3 thanks to the classical four probes experiment.

$$R_1 = R_{C1} + R_{sub1} + R_{C2}$$ **Equation 4.26**

$$R_2 = R_{C2} + R_{sub2} + R_{C3}$$ **Equation 4.27**

$$R_3 = R_{C1} + R_{sub1} + R_{sub2} + R_{C3}$$ **Equation 4.28**

Then, the experimental value of R_E corresponding to the drop of voltage in C_2, it is given by:

$$R_E = \frac{1}{2}.(R_1 + R_2 - R_3)$$ **Equation 4.29**

Whatever the method used for the extraction of the end resistance, the transfer length is always calculated thanks to Equation 4.25 in the case of alloyed contacts.

4.3.5 Limitation of the TLM method

While the TLM method is well adapted for the determination of the specific contact resistivity in the case of ohmic contacts, it presents some limitations when it comes to independently and fully characterizing Schottky contacts. To understand the origin of these restrictions, one must consider the electrical diagram corresponding to the TLM measurements in the case of Schottky contacts (Figure 4.19).

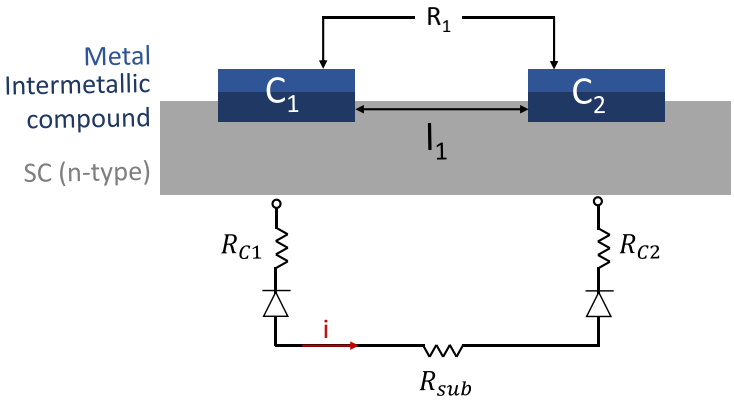


Figure 4.19: Schematic representation of the electrical diagram corresponding to the TLM measurements in the case of Schottky contacts.

While the latter can be considered as pure resistances when they are ohmic (linear I(V) relationship), they behave like diodes coupled with resistances when they are Schottky (cf section 4.2.4). Because both contacts are identical, the TLM's I(V) acquisition is carried out in a "back to back" diodes configuration. As a consequence, whatever the polarization, the current flowing through the overall structure is always limited by the diode operating in reverse mode. In fact, this attribute is exploited by E. Dubois and G. Larrieu to reproduce and characterize the reversed biased junction of a Schottky MOSFET [32]. To summarize, the wholeness of the I(V) characteristic cannot be extracted thanks to this kind of measurement when the contacts are Schottky. The current is underestimated to a certain extent as it corresponds to the reverse part of the I(V) characteristic.

In spite of these limitations, the TLM setup is an easy to integrate and powerful tool enabling the characterization of ohmic contacts. In order to take the most out of it, one must consider the above mentioned limitation and take it into account when exploiting the extracted data.

4.4 Description of the experimental electrical test structures

4.4.1 General presentation of the adopted strategy

As already mentioned, the metallization selected in the frame of the Silicon Photonics must form ohmic contacts with specific contact resistivities lower than 5.10^{-5} Ω.cm² on n-InP and p-InGaAs. While the developments of an innovative contact integration and the associated metallurgical studies have already been covered in chapters 2 and 3, their electrical characterization is yet to be presented. Thus, the following sections will be dedicated to this electrical study thanks to TLM structures, which is itself divided into two main axes, namely:

- The identification of the most suitable Ni and Ti-based metallization(s), *i.e.* deposited metal and subsequent annealing treatment, for the formation of ohmic contacts with low resistivity on n-InP and p-InGaAs;
- The study of the impact of the various dielectric encapsulations presented in section 2.4 on the electrical performances of the contacts.

In order to cover these two axes, the newly developed masks mentioned in chapter 2 and comprising numerous electrical test structures, *i.e.* MELT and TASP, were used. While the two masks address different wafer sizes (respectively 50 to 100 mm and 200 mm), the two of them are comprised of three levels of integration:

- ACTIVE level, used to pattern the semiconductor, *i.e.* the III-V stacks, and limit the crowding effect;
- CONTACT level, used to pattern the contact cavities were the Si-microelectronics compatible metallization is integrated;
- METAL level, used to integrate metallic pads necessary to polarize the contact test structures during the electrical characterization.

The mask TASP was mainly used to develop the integration of the contacts in a 200 mm Si-compatible clean room presented in Chapter 2. The development of this integration scheme required numerous sub-studies, and thus lasted not less than 2 years. Because the fact that this development would require several years was known, a second mask, MELT, was developed to conduct upstream electrical characterizations. This approach presents various advantages:

- The integration scheme used with the mask MELT is similar to TASP's but is simplified. The time needed to perform the overall integration is therefore less important and a wide range of metallizations and dielectric compounds can be probed.
- A first electrical characterization of the contacts could be performed in parallel to the development of the integration scheme in the 200 mm Si-clean room. As a consequence, the most suitable candidates, *i.e.* nature of the deposited metal and subsequent thermal budget, were selected thanks to MELT before being implemented on the 200 mm-wafers.
- The integration of the contacts thanks to the mask MELT could be realized on samples (quarters of 2-inches wafers for example) rather than on wafers. Because the III-V materials are quite expensive, this attribute is of great interest in the first stages of the materials' selection.

Therefore, the results presented in this section will correspond exclusively to the ones obtained with the mask MELT.

4.4.2 Description of the electrical test structures (MELT)

As already mentioned, the mask MELT is dedicated to the patterning of electrical test structures on III-V wafers whose diameters range from 50 mm to 100 mm. The electrical test structures present on this mask are exclusively composed of TLM, either linear or circular (CTLM). The layout corresponding to the three lithography levels stacked is presented in Figure 4.20.

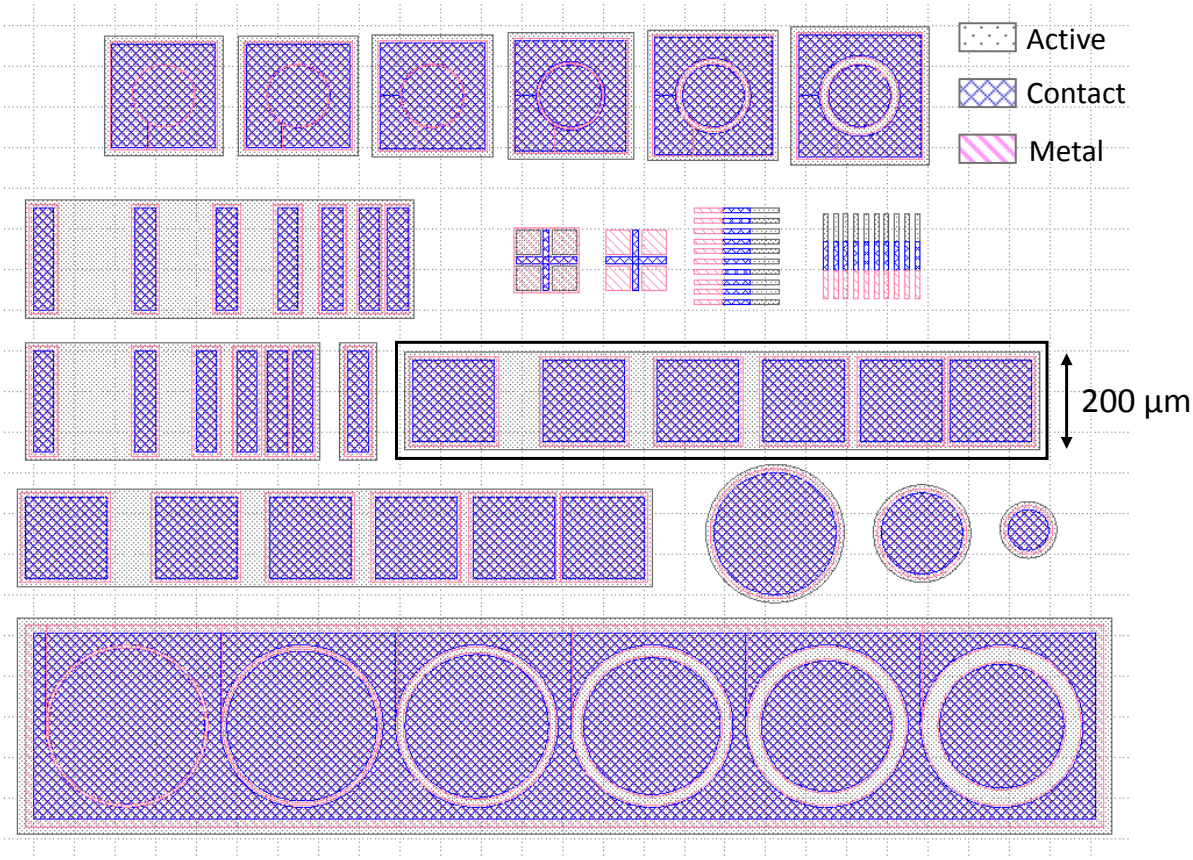


Figure 4.20: Layout of the mask MELT displaying the three levels of integration. The black rectangle highlights the linear TLM structure used for the extraction of the results presented in this chapter.

The black rectangle frames the linear TLM used for the extraction of the results presented in this chapter. The latter is composed of squared contacts (a = W = 200 µm) separated by spacings ranging from 20 µm to 120 µm as detailed in Figure 4.21.

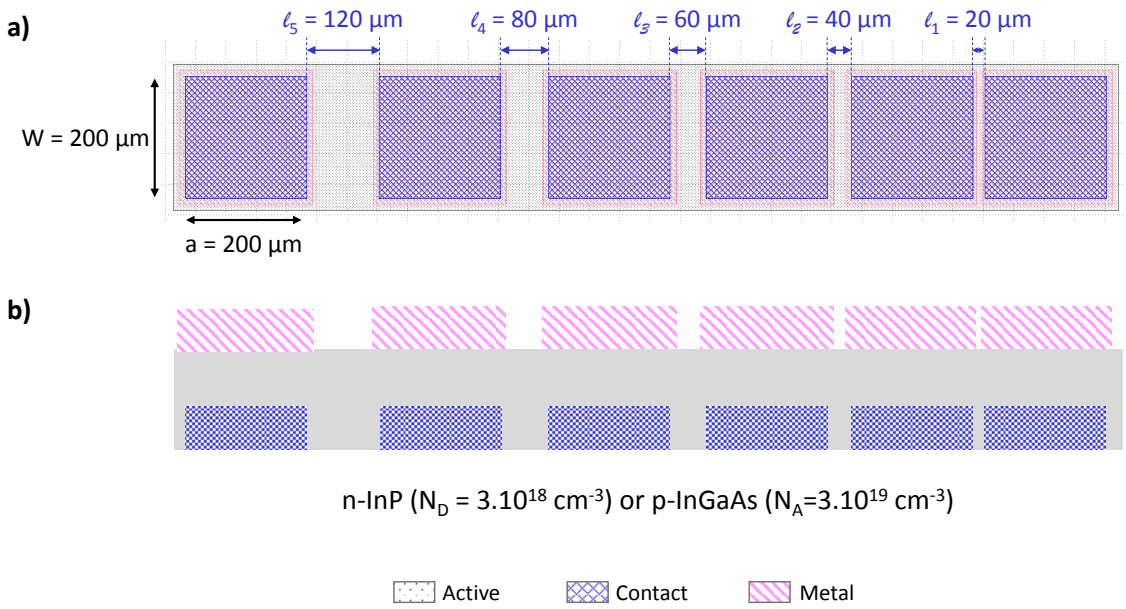


Figure 4.21: Zoom-in of the TLM structure used for the extraction of the electrical results presented in this chapter – (a) top view and (b) cross section.

The measurement procedure corresponds to the one detailed in section 4.3: the adjacent contacts are probed thanks to a four probes setup to extract the corresponding I(V) characteristics. More precisely, a current generator provides the intensity required to obtain a drop of voltage ranging from about -1 V to +1 V in the overall structure. In the meantime, a voltmeter measures the actual drop of voltage as the latter can differ from the targeted value. This situation occurs when the current compliance used to limit the DC current, and therefore prevent any damage to the structures, is reached. Note that this step of data acquisition and the following resistance extraction are always repeated on nine different chips in order to test the reproducibility of the results. In the case of non-linear relationship between the voltage and the current, the contact is declared as being Schottky; otherwise, the corresponding resistance is extracted thanks to two different methods[6].

(i) The first method consists in calculating the resistance corresponding to each probed point, *i.e.* to each probed I-V couple. These calculations are conducted for the five spacings, and always repeated on nine chips. To do so, a first filter is applied to eliminate the measurement errors that often occur when the current and the drop of voltage are too small. This filter consists in suppressing the negative resistances along with the ones that are way higher than the mean value (for example, when the mean value is of 10 Ω, all resistances below 0 Ω and above 100 Ω are not taken into

[6] Note that in order to determine if the contacts were ohmic or Schottky, additional I(V) extractions were conducted on CTLM structures. Indeed, the latter enable a minimization of the substrate's contribution compared to the linear TLM on MELT as they present lower spacings.

account). The filtered mean value is then calculated along with the corresponding standard deviation.

(ii) The second method exploits the plotting of the I(V) curves. By taking the inverse of their slope, one can access the mean value of the resistance, therefore disregarding the measurement errors provided that the correlation coefficient is close to 1.

The two methods have always been used for the extraction of the specific contact resistivities and gave very close results. Therefore, for the sake of simplicity and because it does not take into account isolated measurement errors, the results presented in the following will be solely based on the second method.

4.5 Electrical characterization of the Si-compatible Ni and Ti-based metallizations

As briefly detailed in the previous section, the electrical characterization of the contacts covers two main axes, the first one of them being the study of the Ni and Ti-based Si-compatible metallizations presented in Chapter 3. This electrical study aims to determine which metallization(s) and subsequent thermal treatment(s) is/are the most suitable on both surfaces of interest, *i.e.*, n-InP and p-InGaAs.

4.5.1 Experimental procedure

The experimental procedure followed for the integration of these systems firstly includes a III-V surface preparation in a diluted HCl solution (HCl : H_2O = 1 : 10). In order to be consistent with the contacts' integration presented in Chapter 2, a layer corresponding to the hard mask used for the patterning of the III-V is then deposited. The latter is composed of the conformal SiN and is 50 nm thick. Again, similarly to Chapter 2, the 150 nm-thick top layer is composed of SiO_2 deposited at 300 °C. The contact lithography level is then used in order to pattern contact cavities in this dielectric stack. The etching of these compounds down to the III-V surfaces is achieved thanks to a dry SF_6-based plasma. After the definition of the contact cavities, the III-V wafers are once again dipped into the diluted HCl solution in order to remove all particles and oxides from the surface. Because an air break is inevitable, an Ar^+ plasma pre clean is conducted right before the deposition of the various metallizations. Some samples were deliberately not submitted to this Ar^+ preclean in order to probe the impact of its presence / absence on the electrical characteristics of the contacts. The 20 nm – thick Ni and the Ti layers are both deposited by PVD respectively at room temperature and 100 °C on

separated samples. Additionally to these two metals, a Ni_2P target was specially designed and ordered for this study. Indeed, very good results were reported in the literature with this metallization on n-InP ($\rho_C = 3 \times 10^{-6}$ Ω.cm^2) and p-InGaAs ($\rho_C = 2 \times 10^{-5}$ Ω.cm^2) while we showed in section 3.4 that is very unlikely to isolate this compound when formed by reaction between a Ni film and the InP substrate [33-35]. All samples are finally encapsulated by a 7 nm-thick TiN capping layer deposited at 100 °C and by a probing layer composed of Au. In order to enable the creation of intermetallic compounds, some sample underwent RTP thermal treatments under N_2 ambient. The annealing temperatures and durations were chosen in the light of the various results reported in Chapter 2 and are detailed in Table 4.1. At this point, the metallization is patterned down to the dielectric stack thanks to the metal lithography level. The final integration step consists in patterning the III-V active epitaxy in order to confine the current streamlines and therefore limit the crowding effect. This patterning requires the localized removal of the dielectric stacks thanks to the SF_6-based dry etching and the etching of the III-V stacks thanks to wet solutions. The latter are composed of a mixture of HCl and H_3PO_4 for InP layers while they are composed of H_2SO_4, H_2O_2 and H_2O when it comes to etch InGaAs epitaxies.

The samples that were fabricated for the purpose of this study are summarized in Table 4.1.

Table 4.1: Recapitulative chart of the samples fabricated for the electrical study of the Si-compatible metallizations on n-InP and p-InGaAs.

<table>
<tr><td rowspan="2">Active epitaxy</td><td>n-InP</td><td colspan="4">X</td><td colspan="4">X</td><td colspan="3">X</td><td colspan="3">X</td><td colspan="4"></td><td colspan="4"></td><td colspan="3"></td><td colspan="3"></td></tr>
<tr><td>p-InGaAs</td><td colspan="4"></td><td colspan="4"></td><td colspan="3"></td><td colspan="3"></td><td colspan="4">X</td><td colspan="4">X</td><td colspan="3">X</td><td colspan="3">X</td></tr>
<tr><td>Integration</td><td>Planar</td><td colspan="4">X</td><td colspan="4">X</td><td colspan="3">X</td><td colspan="3">X</td><td colspan="4">X</td><td colspan="4">X</td><td colspan="3">X</td><td colspan="3">X</td></tr>
<tr><td>In situ Ar+ pre clean</td><td></td><td colspan="4">X</td><td colspan="4">X</td><td colspan="3">X</td><td colspan="3"></td><td colspan="4">X</td><td colspan="4">X</td><td colspan="3">X</td><td colspan="3"></td></tr>
<tr><td rowspan="3">Deposited metallization</td><td>Ni</td><td colspan="4">X</td><td colspan="4"></td><td colspan="3"></td><td colspan="3"></td><td colspan="4">X</td><td colspan="4"></td><td colspan="3"></td><td colspan="3"></td></tr>
<tr><td>Ti</td><td colspan="4"></td><td colspan="4">X</td><td colspan="3"></td><td colspan="3"></td><td colspan="4"></td><td colspan="4">X</td><td colspan="3"></td><td colspan="3"></td></tr>
<tr><td>Ni_2P</td><td colspan="4"></td><td colspan="4"></td><td colspan="3">X</td><td colspan="3">X</td><td colspan="4"></td><td colspan="4"></td><td colspan="3">X</td><td colspan="3">X</td></tr>
<tr><td rowspan="7">Thermal treatment</td><td>None</td><td>X</td><td></td><td></td><td></td><td>X</td><td></td><td></td><td></td><td>X</td><td></td><td></td><td>X</td><td></td><td></td><td>X</td><td></td><td></td><td></td><td>X</td><td></td><td></td><td></td><td>X</td><td></td><td></td><td>X</td><td></td><td></td></tr>
<tr><td>250 °C – 60 s</td><td></td><td></td><td></td><td></td><td></td><td>X</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td>X</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td>300 °C – 3 min</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td>X</td><td></td><td></td><td>X</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td>X</td><td></td><td></td><td>X</td><td></td></tr>
<tr><td>340 °C - 60 s</td><td></td><td>X</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td>350 °C - 60 s</td><td></td><td></td><td>X</td><td></td><td></td><td></td><td>X</td><td></td><td></td><td></td><td>X</td><td></td><td></td><td>X</td><td></td><td>X</td><td></td><td></td><td></td><td></td><td>X</td><td></td><td></td><td></td><td>X</td><td></td><td></td><td>X</td></tr>
<tr><td>450 °C – 60 s</td><td></td><td></td><td></td><td>X</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td>X</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td></tr>
<tr><td>550 °C – 60 s</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td>X</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td>X</td><td></td><td></td><td></td><td>X</td><td></td><td></td><td></td><td></td><td></td><td></td></tr>
</table>

When experimentally extracting the specific contact resistivity on these samples, three limit and characteristic cases were encountered. For the sake of clarity, the latter will be presented in the following based on three representative samples: (i) the Ti/InP system annealed at 550 °C for 60

seconds, (ii) the as deposited Ni_2P/InP and finally (iii) the Ni/InGaAs system annealed at 350 °C for 60 seconds.

4.5.2 Experimental extraction of the specific contact resistivity – Schottky contact

As described above, the first step of these experiments always consists in acquiring the I(V) curves corresponding to each spacing on nine different chips. Figure 4.22 presents the I(V) curves corresponding to one chip of the Ti/InP system annealed at 550 °C for 60 seconds.

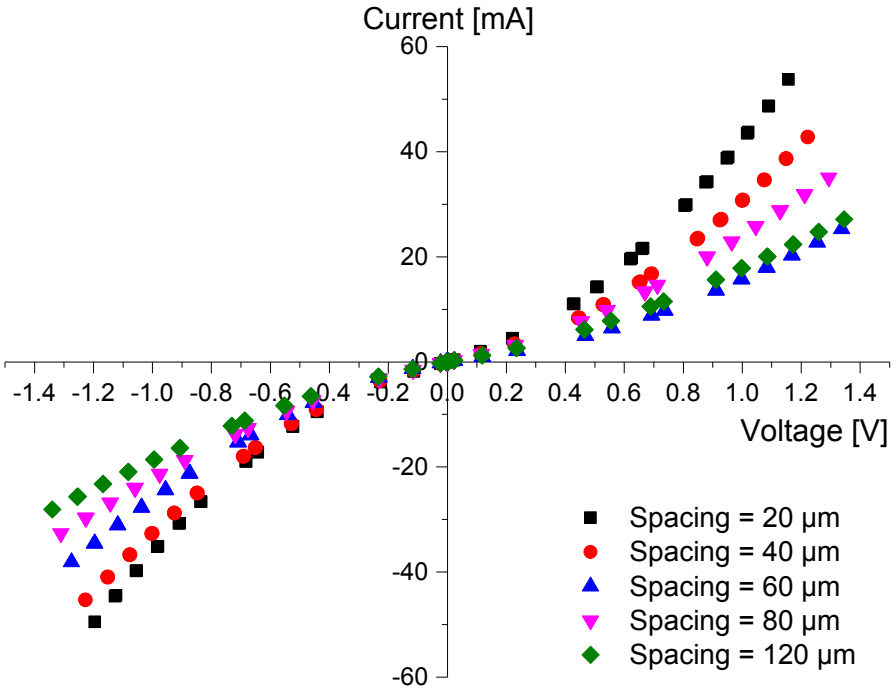


Figure 4.22: I(V) curves corresponding to each spacing of the Ti/InP system annealed at 550 °C for 60 seconds.

One can notice that the I(V) characteristics do not display a linear trend, therefore highlighting the Schottky nature of the contacts. As theoretically expected, the curves tend to recover a linear trend when the contribution of the substrate is maximized, i.e. when the spacing increases. Anyhow, because the contacts are Schottky, their resistance depends on the applied voltage and no quantitative extraction is conducted on this first type of system.

4.5.3 Experimental extraction of the specific contact resistivity – Non-alloyed ohmic contact

The second typical data treatment corresponds to the case of the as deposited Ni_2P/InP system. Figure 4.23 displays the I(V) curves corresponding to every spacing present on one chip. One can notice the linear behavior of all the characteristics, and most importantly, of the one corresponding to the smallest spacing. As expected, the resistance increases with the distance as the contribution of the semiconductor, R_{sub} becomes more and more important.

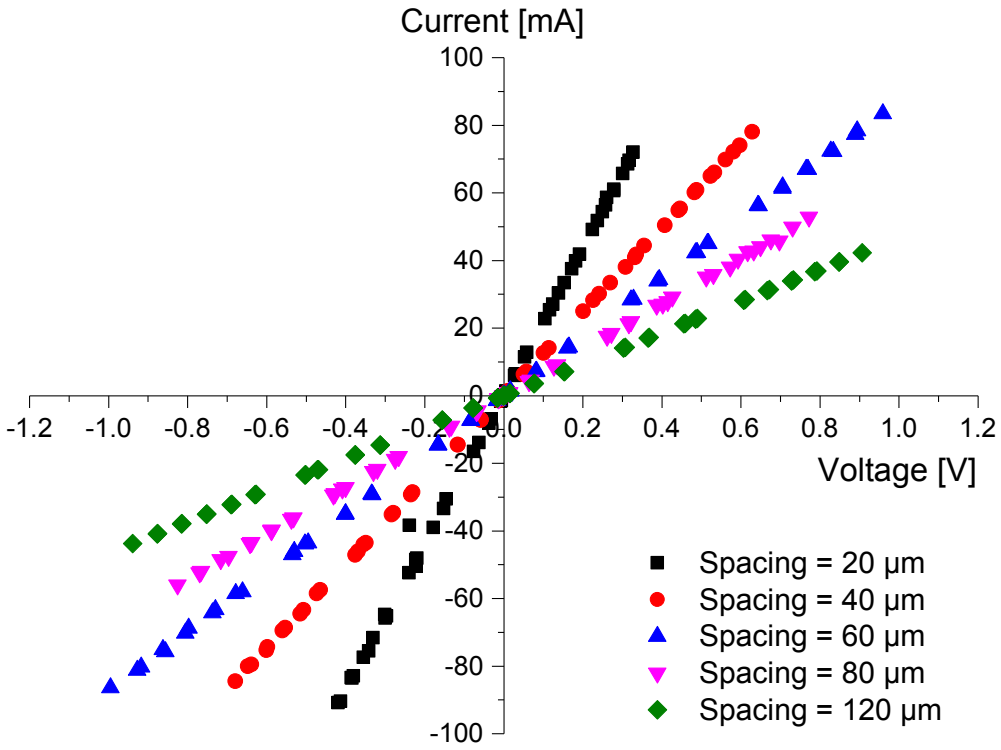


Figure 4.23:I(V) curves corresponding to each spacing of the as deposited Ni_2P/n-InP system.

Contrary to the above mentioned case, these contacts therefore exhibit an ohmic behavior and a quantitative extraction of the specific contact resistivity can be conducted. To do so, the nine resistances corresponding to each spacing are calculated, averaged and plotted as a function of the spacings (Figure 4.24). The linear trend displayed on this plot reflects an efficient confinement of the current streamlines within the active semiconductor region, and therefore a very limited crowding

effect. Moreover, the errors bars displayed on the chart[7] highlight the small deviation existing between the nine chips, and therefore the suitable reproducibility of the measurements.

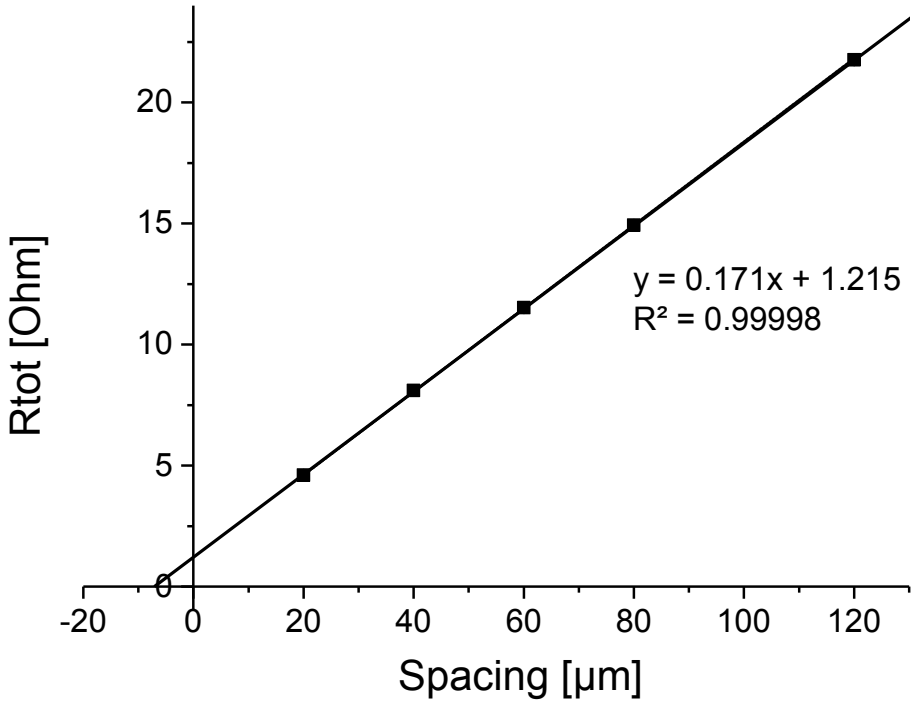


Figure 4.24: Plot of the total resistance measured thanks to the TLM setup as a function of the spacings for the as deposited Ni_2P/n-InP.

The contacts being non-alloyed, no end resistance extraction was necessary and thus conducted. The transfer length, the contact resistance and finally the specific contact resistance are respectively extracted thanks to Equation 4.17, Equation 4.18 and Equation 4.22. The corresponding results are summarized in Table 4.2.

Table 4.2: Recapitulative table of the results obtained on the as deposited Ni_2P/n-InP system

Parameter	Extracted Value
Transfer length $\boldsymbol{L_T}$	3.55 µm
Contact resistance $\boldsymbol{R_C}$	0.61 Ω
Specific contact resistivity $\boldsymbol{\rho_C}$	4.31 x 10^{-6} Ω.cm^2

[7] The error bars are actually contained in the points displayed on the chart. Note that the dispersion mainly emanates from the multiplication of the measurements and not from the actual I and V acquisition themselves.

4.5.4 Experimental extraction of the specific contact resistivity – Alloyed ohmic contact

The last case presented here corresponds to the Ni/InGaAs sample annealed at 350 °C for 60 seconds. The latter displays linear I(V) curves which enables a quantitative extraction of the specific contact resistivity (Figure 4.).

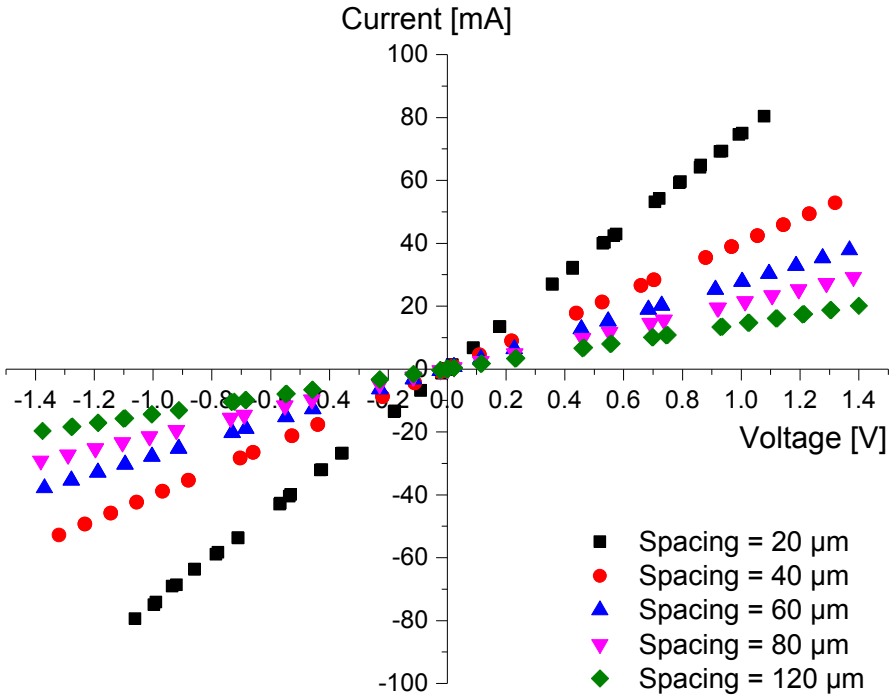


Figure 4.25: I(V) curves corresponding to each spacing of the Ni/InGaAs system annealed at 350 °C for 60 seconds.

However, according to literature, because this sample underwent a thermal treatment the data extraction should be adapted. As detailed in section 4.3.4, the formation of the intermetallic compounds at the metal/semiconductor interface might modify the electrical properties of the semiconductor beneath the contact region. As a consequence, R_{SH} and R_{SK} differ and the transfer length cannot be extracted graphically. As a consequence, the end resistance, R_E, must be determined and the actual transfer length calculated (see section 4.3.4). Apart from this additional step, the specific contact resistivity extraction is identical to the one described above.

The determination of the end resistance was conducted thanks to the two setups described in section 4.3.4.

- The first one, consisting in injecting a current between the first two pads and measuring the resulting drop of voltage between the second and the third pads will be noted “setup A” (Figure 4.17).
- The second one, which consists in measuring the resistances corresponding to three adjacent pads, R_1, R_2 and R_3 will be noted “setup B” (Figure 4.18).

Extraction of the end resistance thanks to *Setup A*

Setup A was firstly used for the extraction of the end resistance on the Ni/InP sample annealed at 340 °C for 60 seconds. In order to test this measurement configuration, several sets of contacts were probed: a first set of measurements was performed by injecting the current between contacts 1 and 2 and measuring the drop of voltage between pads 2 and 3; a second was similarly performed between pads 3, 4 and 5 (Figure 4.26).

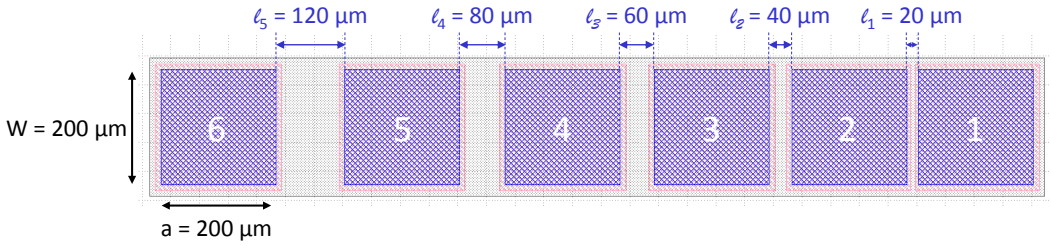


Figure 4.26: Layout of the TLM structure used for the end resistance measurements.

Unfortunately, this kind of measurement provided unreliable results. Indeed, while several measurements were performed on the same set of contacts, the obtained results were not reproducible from one chip to another. Moreover, changing the set of contacts that were probed led to a modification of the extracted value, indicating that not only the end resistance was measured. Oddly enough, these kinds of limitations are not discussed in articles dealing with linear TLM while they are mentioned in the case of Circular TLM (CTLM) [36-39]. Yet, the final measurement configuration is the same when observed in cross section, as represented in Figure 4.27.

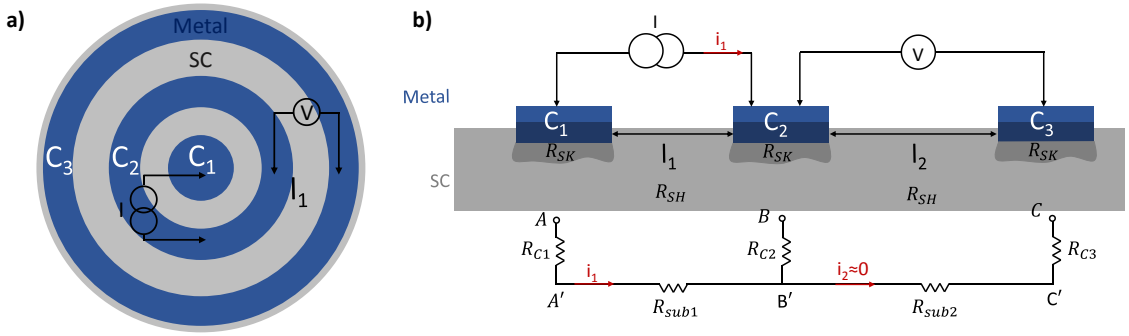


Figure 4.27: (a) Schematic representation of the end resistance extraction on CTLM and (b) corresponding electrical diagram.

In order to identify the origins of these parasitic resistances, one must consider the basis of this data extraction. The determination of the end resistance relies on the fact that no current is flowing from point B to point C. Thus, the measured drop of voltage should correspond solely to the one occurring in contact C_2, *i.e.* between points B and B'. However, in practice this hypothesis might not be respected. Alok *et al* and Connelly *et al* showed that a drop of voltage actually occurs between points B' and C' when a current is flowing between contacts C_1 and C_2 (Figure 4.28) [37, 40]. Therefore, the overall drop of voltage measured thanks to this setup results not only from the end resistance, but also from the contribution of the semiconductor located between C_2 and C_3. To minimize the latter contribution, a diminution of its thickness compared to the spacings is necessary. Thanks to this precaution, a confinement of the isopotential lines is achieved vertically and as a consequence laterally. Nonetheless, this kind of measurement is only valid if the sheet resistance of the semiconductor is low compared to the value of the end resistance, *i.e.* if the transfer length is important enough. Otherwise, the actual value of the end resistance is entirely hidden by the substrate's contribution. As a consequence, because the experimental results were found as being unreliable, as supported by literature, the second measurement method was probed.

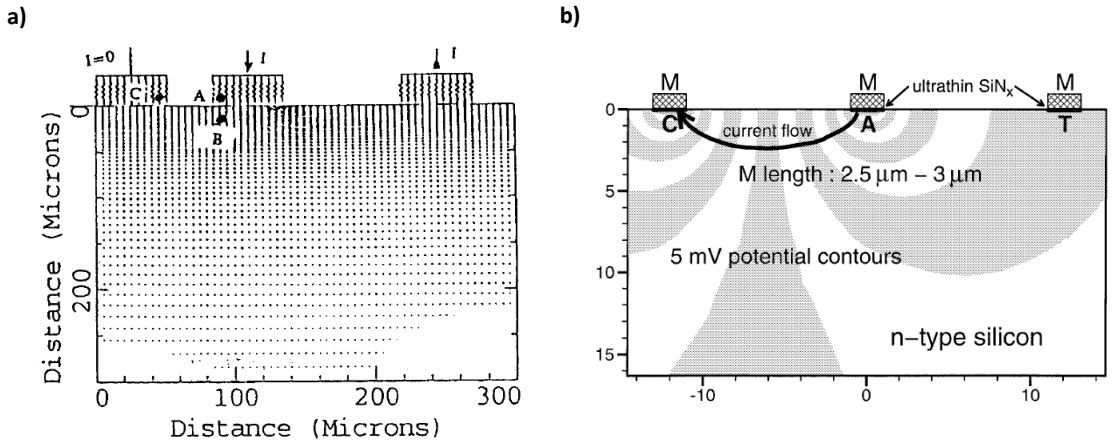


Figure 4.28: (a) Current distribution in the case of a bulk semiconductor region obtained using numerical simulation [37] and (b) Schematic cross section of a metal/n-type Si junction structure highlighting the presence of isopential lines between two contacts that are not polarized [40].

Extraction of the end resistance thanks to *Setup B*

The second method relies on the measurement of three different resistances thanks to a four probe setup (Figure 4.18). Here again, several measurements were conducted on several set of contacts in order to test the reproducibility of the end resistance extraction. In Table 4.3, the results obtained on the Ni/InP sample annealed at 340 °C for 60 seconds are listed for the three sets of contacts that were probed.

Table 4.3: Values of R_1, R_2, R_3 and R_E extracted using setup B on the Ni/InP sample annealed at 340 °C for 60 seconds

Set of contacts probed	R_1	R_2	R_3	R_E
Contacts 1 2 3	6.38 Ω	10.11 Ω	16.38 Ω	0.06 Ω
Contacts 3 4 5	13.76 Ω	17.40 Ω	31.47 Ω	-0.15 Ω
Contacts 4 5 6	17.40 Ω	24.47 Ω	42.02 Ω	-0.07 Ω

As displayed, the values of R_E strongly depend on the set of contacts that are probed. Even more surprisingly, two out of the three sets lead to negative end resistance values. Obviously, this kind of result is physically impossible and highlights a weakness in this extraction process. Although no such theory has already been reported, the drawing of the electrical diagram, taking into account the transfer length, gives an insightful perspective (Figure 4.29).

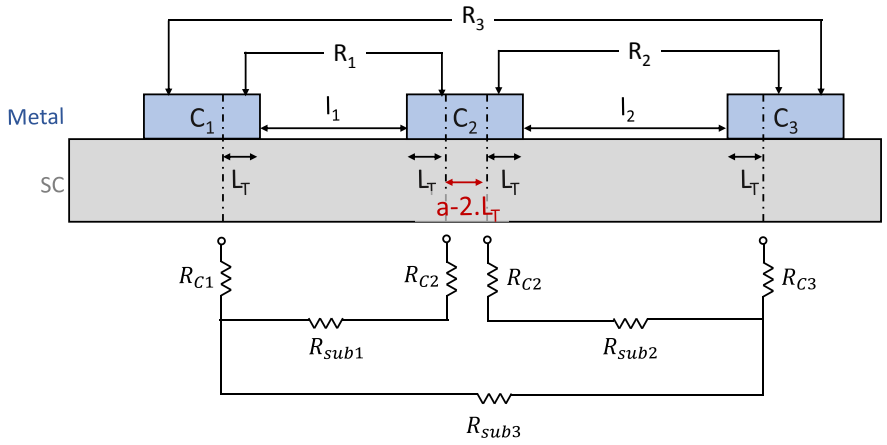


Figure 4.29: Electrical diagram corresponding to the setup used for the extraction of R_E taking into account the transfer length.

As schematized in Figure 4.29, considering the transfer length modifies the equations classically used for the extraction of the end resistance (Equation 4.26 to Equation 4.29). Indeed, in this case, the sum of the contributions R_{sub1} and R_{sub2} is not equal to R_{sub3}. In this case, if L_T is small compared to the lateral dimension of the contact a, the end resistance calculated from Equation 4.29 is negative, as observed in the Ni/InP sample annealed at 340 °C for 60 seconds. Therefore, in order to take into account the contribution of the portion represented in red, Equation 4.29 becomes:

$$R_E = \frac{(R_1 + R_2 - R_3)}{2} + \frac{R_{SH}.(a - 2.L_T)}{2.W}$$ [8] **Equation 4.30**

The extraction of the transfer length is achieved by equalizing the expressions of R_E extracted from Equation 4.25 and Equation 4.30:

$$\frac{R_C}{\cosh(a/L_T)} = \frac{(R_1 + R_2 - R_3)}{2} + \frac{R_{SH}.(a - 2.L_T)}{2.W}$$ **Equation 4.31**

Note that the sheet resistance of the semiconductor is determined graphically thanks to the $R_{tot}(l_x)$ plot, the slope of the curve being equal to R_{SH}/W.

This data treatment was applied to several annealed samples[9] and provided without exception the same result. The transfer length always oscillates between 98 µm and 99 µm while the resulting specific contact resistivity ranges from $1x10^{-4}$ Ω.cm^2 to $3.5x10^{-4}$ Ω.cm^2. The similarity of all these results, yet obtained on very different samples raised questions about the validity of these extractions. In order to further test this method, it was applied to the as deposited Ni_2P/InGaAs sample, the aim being to compare these results to the ones obtained with the extraction method classically used for non-alloyed systems. Figure 4.30 shows the TEM cross sections corresponding to this sample along with the spatial repartition of the elements. The latter indicates that the layers are fully intact and that no interdiffusion occurred. Therefore, one can reasonably assume that the sheet resistance of the semiconductor is not modified underneath the contact regions and that the two extraction methods should provide comparable results.

[8] Note that, depending on the path followed by the charge carriers, R_{SH}might have to be replaced by R_{SK}. This path for example depends on the redistribution of the doping species underneath the contact region (depletion / accumulation).

[9] The updated extraction was applied to the Ni/InP sample annealed at 340 °C and 350 °C, the Ni_2P/InP system annealed at 300 °C and 350 °C and the Ni/InGaAs sample annealed at 350 °C and 450 °C.

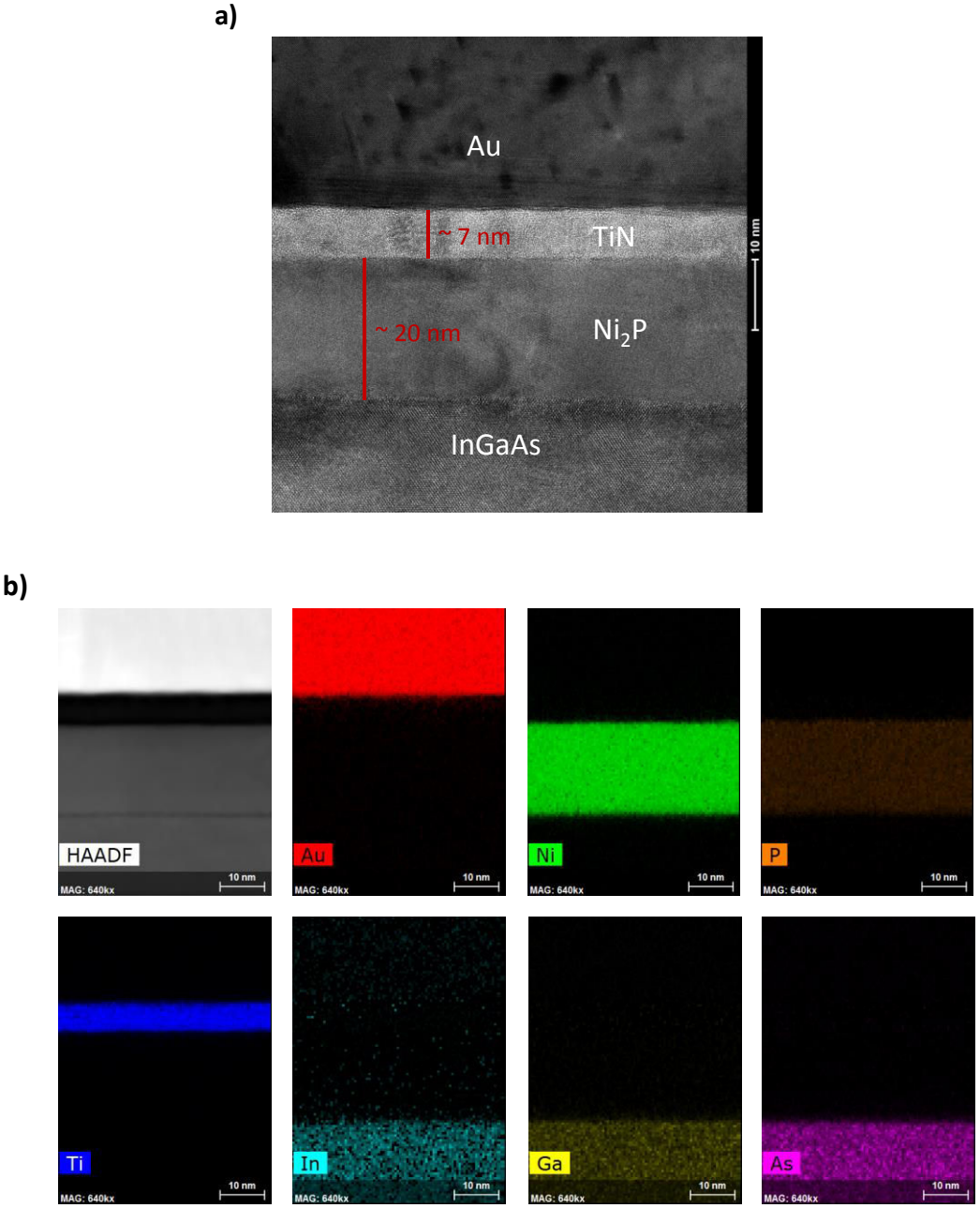


Figure 4.30: (a) TEM cross section of the as deposition Ni_2P/InGaAs and (b) spatial repartition of the elements present in the system.

Yet, both methods provide very different results as displayed in Table 4.4. The most remarkable point concerns the fact that the ones obtained thanks to the updated *setup B* are once again similar to the ones extracted for all the annealed samples.

Table 4.4: Recapitulative table of the results obtained on the as deposited Ni_2P/InGaAs sample

	L_T	ρ_C
"Non-alloyed" extraction method	3.29 µm	1.23 x 10^{-5} Ω.cm^2
Updated setup B for alloyed contacts	99.87 µm	3.56 x 10^{-4} Ω.cm^2

Based on these various results, it seems the extraction of the end resistance R_E is far from being trivial. Even in its updated version, *setup B* presents some limitations that could be linked to several phenomena[10].

First of all, in Equation 4.31, we assume that the charge carriers travel solely through the bulk semiconductor once they have passed the contact interface. However, the end resistance extraction is conducted for the only purpose of taking into account the modification of the semiconductor's sheet resistance underneath the contact region. To counteract this approximation, one could partially substitute the value R_{SH} by R_{SK}. The difficulty lies in the determination of the path followed by the current and therefore the distances over which the sheet resistance is equal to R_{SH} and to R_{SK}. Two extreme situations can occur, as represented in Figure 4.31. In the case depicted in Figure 4.31(a), the distance over which the semiconductor's sheet resistance is equal to R_{SK} is roughly twice the transfer length. However, if the modified sheet resistance, R_{SK}, is less important than the bulk one, R_{SH}, the charge carriers might modify their path underneath C_2 as represented in Figure 4.31(b). In this case, because the region where the sheet resistance is equal to R_{SK} is thinner than the bulk semiconductor, a shrinking resistance might appear. The path ultimately followed by the charge carriers will then result from a competition between the specific contact resistivity, the bulk and modified sheet resistance of the semiconductor and the potential shrinking resistance. It is therefore very complicated if not impossible to evaluate it without additional theoretical simulations.

[10] Note that the list provided along with the associated explanation might not be exhaustive.

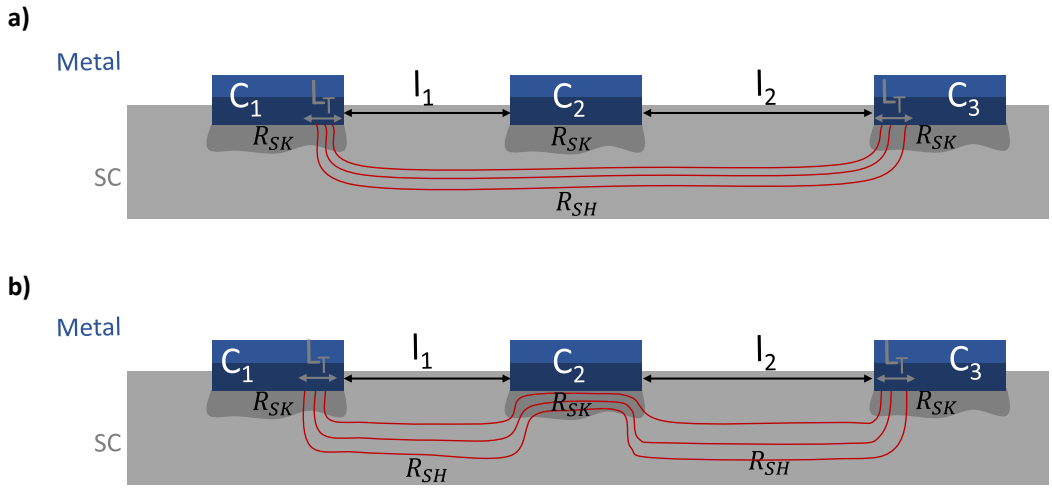


Figure 4.31: Schematic representation of the path that can be followed by the charge carriers during the measurement of R_3.

On top of that, utilizing this updated extraction method is efficient over a limited range of contact resistance versus semiconductor sheet resistance ratio. Indeed, in systems presenting very small transfer lengths compared to the dimensions of the contacts, the charge carriers might go back in contact C_2 during the measurement of R_3. This attribute is for example exploited by Yu *et al.* for the determination of ultralow contact resistivities ($\rho_C < 10^{-8}$ Ω.cm^2) thanks to a multiring CTLM setup [41]. If this situation actually occurs, the value of the end resistance cannot be extracted thanks to this setup. The whole issue lies in the determination of the critical transfer length from which the charge carriers would benefit from going back in C_2 rather than staying in the semiconductor during the measurement of R_3. If one considers only the definition of the transfer length, one would expect this situation to occur as soon as L_T is smaller than the length of the contact a. However, because the contact C_2 is not polarized during the measurement of R_3, theoretical simulations would be once again of great interest to predict the path actually followed by the charge carriers during this measurement.

Considering these results, it seems that this kind of measurement presents strong limitations even in its upgraded version when arrays of contacts are probed[11]. Unfortunately, the reliability of the obtained results appears to be highly questionable. As a consequence, the results presented in the next section will exclusively emanate from the extraction method classically used for non-alloyed systems. Even though the contact resistivities might be somehow underestimated for the annealed samples, they will provide an accurate trend allowing us to identify the most suitable metallizations and thermal treatments.

[11] In order not to encounter the above mentioned restrictions, optimized and decoupled structures were implemented on the 200 mm mask that was developed (TASP). The values of R_1, R_2 and R_3 can be independently measured on three separated sets of contacts thanks to these structures.

4.5.5 Electrical characterization of Si-compatible metallizations on n-InP

The extraction method described in section 4.5.3 was therefore applied to the integrality of the samples presented in Table 4.1. For the sake of clarity, the results obtained on n-InP and p-InGaAs will be presented and discussed separately. The next section will be therefore dedicated to those obtained on n-InP surfaces (N_D = 3 x 10^{18}cm^{-3}), the latter being summarized in Figure 4.32. Taking into account the uncertainties arising from the I(V) measurement itself, from the measurement of the contacts' dimensions, from the linear regressions and from the reproducibility of the measurements on the nine chips, the error linked to the extracted was calculated. All results presented in the next sections are therefore given with the precision $\Delta\rho_C/\rho_C = 3.10^{-2}$.

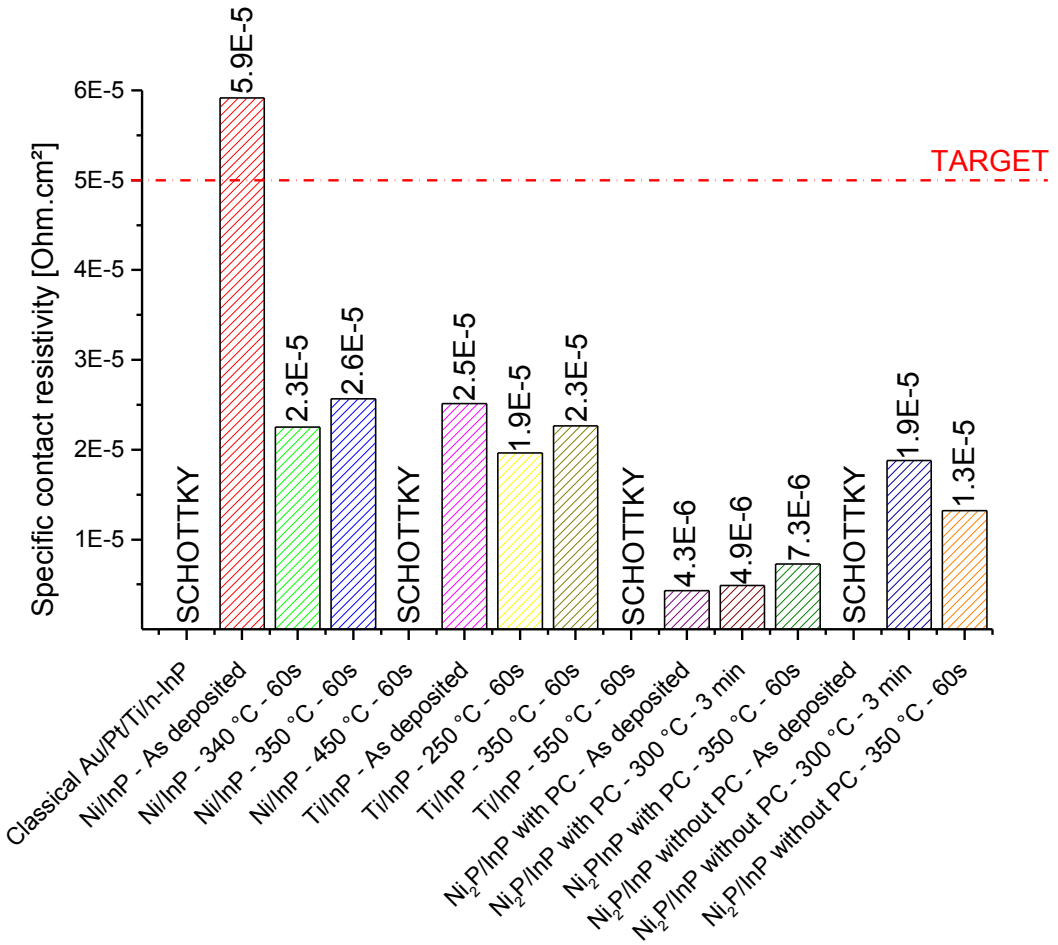


Figure 4.32: Specific contact resistivities of Ni and Ti-based metallizations to n-InP (N_D = 3 x 10^{18} cm^{-3}). When encountered, PC stands for in situ Ar^+ pre clean.

It appears that most the of metallizations present specific contact resistivities meeting the target in terms of specific contact resistivity which is fixed at 5 x 10^{-5} Ω.cm^2. Moreover, the great majority of them present better electrical characteristics than the classical Au/Pt/Ti metallization which is

Schottky on n-InP when integrated thanks to a Si-compatible integration scheme. However, while some thermal treatments lead to an enhancement of the conduction through the metal/semiconductor, some strongly deteriorate it. These electrical evolutions being linked to the modification of the composition and morphology of the systems, a particular attention will be paid to link these various characteristics.

While the as deposited Ni does not provide satisfying results, the specific contact resistivity drops under the target after an annealing treatment conducted at 340 °C for 60 seconds. In section 3.4, XRD characterizations conducted on this system highlighted the co-existence of binary and ternary phases at this temperature, namely Ni_2P, Ni_3P and Ni_2InP, while the as deposited sample was only composed of crystalline Ni and of an amorphous α-Ni-In-P layer. Therefore, it appears that the formation of these three phases is electrically favorable on n-InP. Moreover, the XRD also featured the appearance of the In phase consequently to a 10 °C temperature rise. The associated TEM cross sections however did not feature the presence of isolated In grains, suggesting that this phenomenon might only be initiated at 350 °C. In order to observe if the appearance of the In phase had an impact on the electrical properties of the contact, the corresponding system was probed. However, it seems that the contact resistivity is not much impacted as it only increases from 2.3×10^{-5} Ω.cm^2 to 2.6×10^{-5} Ω.cm^2. On the contrary, a 100 °C increase in temperature lead to an important degradation of the contacts that became Schottky at 450 °C. We saw in section 3.4 that the samples feature comparable compositions from 300 °C to 450 °C. As a consequence, the nature of the phases which initially lead to an improvement of the electrical properties of the contact does not seem to be responsible for this degradation. It is therefore reasonable to hypothesize that the thermal treatment conducted at 450 °C resulted in the initiation of the layers' morphology degradation and/or to an agglomeration of the compounds. This hypothesis is supported by the TEM cross section conducted at 550 °C on which the Ni_2P was found to be fully agglomerated and surrounded by the In phase. In conclusion, in order to minimize the specific contact resistivity while avoiding the formation of the In phase which might lead to non-reproducible results, the formation of Ni-based contacts to n-InP surfaces must be realized at temperatures that do not exceed 340 °C.

The Ti metallization presents even more strict restrictions concerning the maximum acceptable temperature. Indeed, while it is perfectly ohmic after deposition and after a thermal treatment at 250 °C, a degradation of the electrical properties occurs at higher temperatures. The contact resistivity starts to increase at 350 °C and the contact displays a marked Schottky behavior after the annealing treatment conducted at 550 °C as displayed in Figure 4.33. However, it seems that this change of behavior initiated at 350 °C is not linked to a modification of the system's composition. Indeed, the corresponding XRD characterizations (see section 3.8) showed that the composition of the systems is stable from deposition to 450 °C (co-existence of Ti_2In_5, TiP and Ti). Therefore, once

again, the modification of the electrical properties is at least partially linked to a degradation of the system's morphology from 350 °C. It is important to note that annealing treatment conducted at 550 °C is electrically unfavorable, most probably because of a degradation of the system's morphology. As a consequence, in order to form Ti-based ohmic contacts with low specific contact resistance, the intermetallic phases must be formed at low temperature (T ≤ 350 °C).

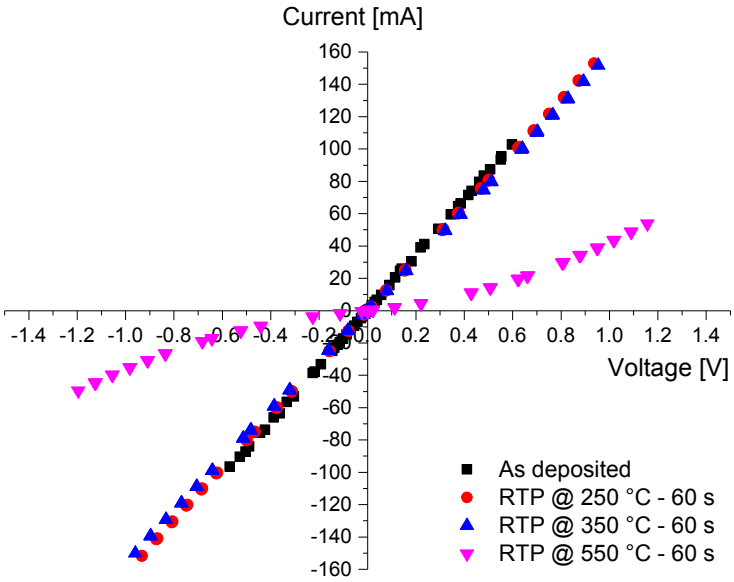


Figure 4.33: I(V) curves corresponding to the lowest spacing (20 µm) of the Ti/n-InP system after deposition and after thermal treatment at 250 °C, 350 °C and 550 °C for 60 seconds.

Finally, the Ni_2P metallization was probed and provided very good and thermally stable results when its deposition is preceded by an in situ Ar^+ pre clean. From deposition to 350 °C, the specific contact resistivity oscillates between 4.3 x 10^{-6} Ω.cm^2 and 7.3 x 10^{-6} Ω.cm^2. However, when the dry pre clean is suppressed, the contact becomes Schottky. This result might be surprising as we demonstrated in section 3.4.2 that this kind of in situ treatment strongly degrades the surface morphology when applied to InP. Yet, it allows a suppression of the oxides that regrow during the wafers transfer. Figure 4.32 clearly highlights the fact that the presence of a native oxide is way more detrimental for the electrical performances of the contacts than the modification of the InP surface state. It is important to note that, without pre clean, the specific contact resistivity tends to be lowered subsequently to a thermal treatment. We attribute this to a rearrangement of the species that might occur at Ni_2P/InP interface. Thanks to this mechanism, the oxide layer must become discontinuous if not dissolved into the compounds. Even though the nominal value obtained when a pre clean is conducted is not recovered, these results experimentally highlight the advantages of performing thermal treatments in order to lower the impact of the semiconductor surface state. This kind of solution is therefore of great interest when the semiconductor surface cannot be properly cleaned

right before the deposition process thanks to in situ pre cleans. Note however that a first step of wet cleaning is necessary to limit the thickness of the native oxide on the semiconductor as a too thick layer would inhibit any reaction even during thermal treatments.

Overall, it seems that the Ni_2P metallization combined with an in situ Ar^+ preclean represents the most suitable available solution for the formation of ohmic contacts with a specific contact resistivity as low as 4.3 x 10^{-6} Ω.cm^2 on n-InP. The latter additionally presents the advantage of being stable at least up to 350 °C and could therefore withstand additional processes conducted at this temperature.

4.5.6 Electrical characterization of Si-compatible metallizations on p-InGaAs

Similarly, the above mentioned metallizations were deposited and electrically characterized on p-InGaAs (N_A = 3 x 10^{19} cm^{-3}). The resulting contact resistivities are displayed in Figure 4.34

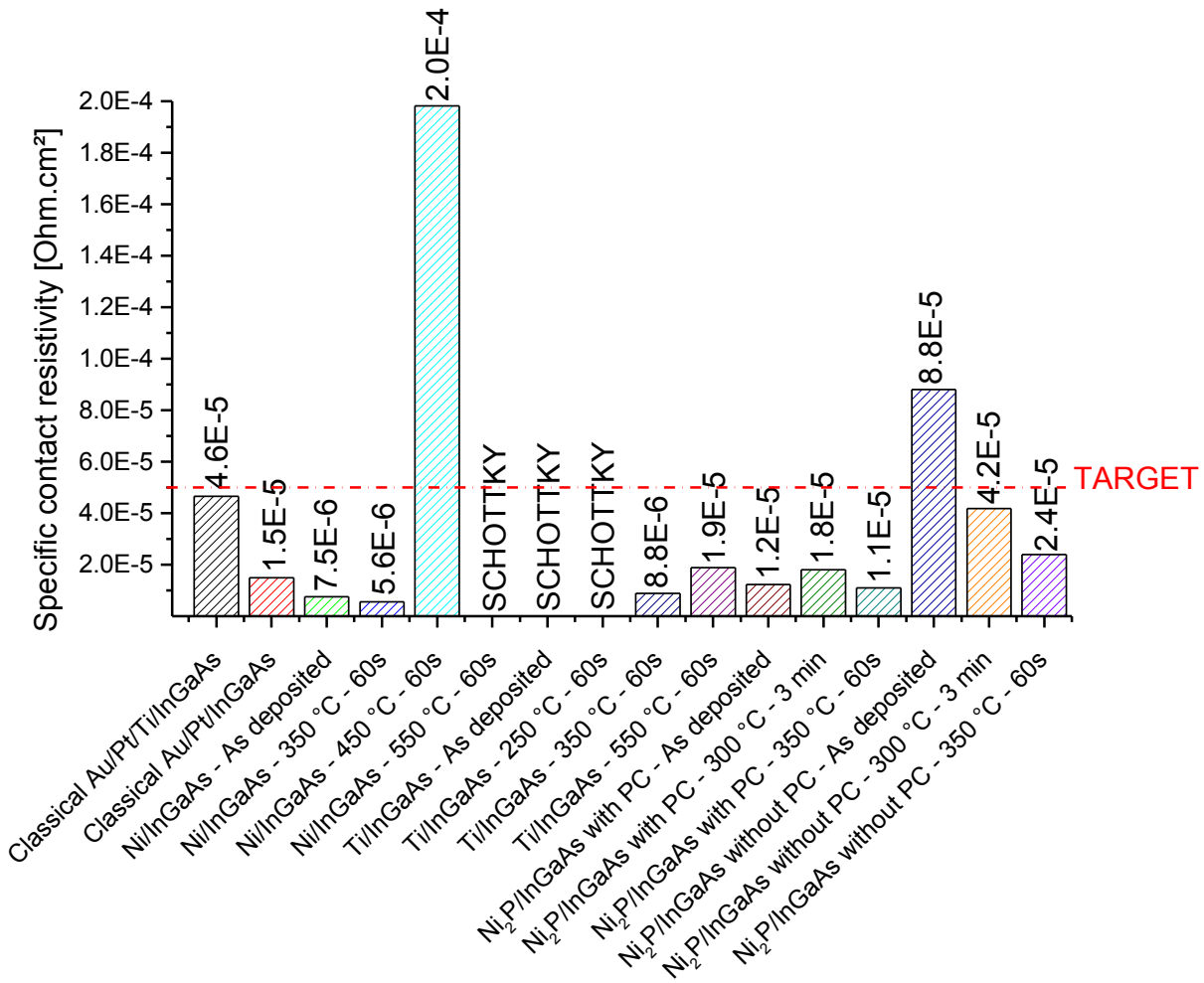


Figure 4.34: Specific contact resistivities of Ni and Ti-based metallizations to p—InGaAs (N_A = 3 x 10^{19} cm^{-3}). When encountered, PC stands for in situ Ar^+ pre clean.

Once again, it appears that most of the metallizations provide electrical characteristics meeting the requirements of the Silicon Photonics requirements ($\rho_C \leq 5 \times 10^{-5}$ Ω.cm^2).

First of all, the as deposited Ni on p-InGaAs presents one of the lowest specific contact resistivities presented in this study on this kind of semiconductor, *i.e.* $\rho_C = 7.5 \times 10^{-6}$ Ω.cm^2. Conducting an annealing treatment at 350 °C for 60 seconds lowers even more this value that reaches 5.6×10^{-6} Ω.cm^2. These results are particularly notable as most studies reported in the literature notify the Schottky nature of the Ni/InGaAs contacts after deposition and after RTP [42-44]. As a consequence, contrary to literature, both the as deposited Ni and the intermetallic compound $Ni_6InGaAs_2$ are electrically very favorable on p-InGaAs. However, these characteristics are degraded from 450 °C where the specific contact resistivity sharply increases. This degradation is confirmed by a transition toward Schottky behavior at 550 °C. This evolution comes as no surprise given the fact that the Ni-InGaAs compound is fully agglomerated at this temperature.

Contrary to all the above mentioned systems, the Ti metallization on p-InGaAs requires temperatures equal to or higher than 350 °C to become ohmic. Right after deposition, the I(V) characteristics present an important curvature that tends to be reduced, along with the associated resistances after the RTP at 250 °C (see Figure 4.35). This positive evolution linked to an increase of the temperature is confirmed by the sample annealed at 350 °C. The latter presents a fully ohmic behavior with a specific resistivity of $\rho_C = 8.8 \times 10^{-6}$ Ω.cm^2 [12]. The XRD characterizations presented in appendix A3 highlighted the initiation of a reaction at 250 °C which is enhanced at 350 °C. As a consequence, although the nature of the compound(s) present from 250 °C to 350 °C could not be determined, they allow the formation of ohmic contacts and are therefore electrically favorable. The formation of the TiAs phase at higher temperatures (T ≥ 450 °C) associated with an In release similarly enables to reach low resistivity values. Although the latter slightly increases after the annealing treatment conducted at 550 °C, it still meets the requirements of the Silicon Photonics ($\rho_C = 1.9 \times 10^{-5}$ Ω.cm^2). The most remarkable attribute of this result lies in the thermal stability of this system which presents a low specific contact resistivity at temperatures as high as 550 °C. This important thermal stability is of great interest, especially considering the fact that the subsequent integration steps might be realized at temperatures as high as 440 °C (see section 2.7).

[12] Note that when fully integrating the contacts thanks to the innovative scheme presented in Chapter 2, this value is lowered down to 1.7×10^{-6} Ω.cm^2. This first result opens the way towards further lowering the specific contact resistivities thanks to the optimized integration conducted on 200 mm wafers in the Si-compatible clean room.

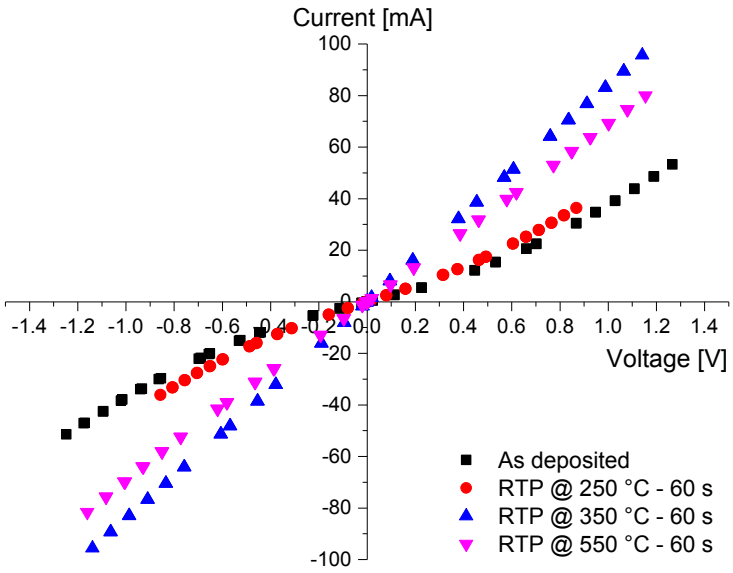


Figure 4.35: I(V) curves corresponding to the lowest spacing (20 µm) of the Ti/p-InGaAs system after deposition and after thermal treatment at 250 °C, 350 °C and 550 °C for 60 seconds.

Finally, the Ni_2P metallization was probed and provided very interesting results when coupled to an Ar^+ preclean, just like it did when deposited on the n-InP surface. Here again, the specific contact resistivity is stable from deposition to 350 °C where it ranges from 121 x 10^{-5} Ω.cm^2 to 1.8 x 10^{-5} Ω.cm^2. However, when the in situ preclean is suppressed, the resistivity strongly increases because of the presence of a native oxide at the interface between the metal and the semiconductor. Performing a thermal treatment leads to a diminution of the contact resistivity indicating the lowered impact of this oxide layer that might become discontinuous.

Overall, the metallizations that would optimize the electrical performances of Si microelectronics compatible contacts to p-InGaAs are:

- The Ni after a thermal treatment conducted at 350 °C for 60 seconds, *i.e.* the $Ni_6InGaAs_2$ phase;
- The Ti after a thermal treatment conducted at 350 °C for 60 seconds;
- The Ni_2P combined with an in situ Ar^+ preclean, this system providing similar results after deposition and after thermal treatments conducted at 300 °C for 3 minutes or at 350 °C for 60 seconds.

4.5.7 Conclusion on the choice of the metallization

Based on the above mentioned results, it appears that many of the probed metallizations could be used to electrically pump the III-V laser. However, the electrical study combined with the metallurgical one give us a very good insight in order to reduce the choices to only a few. The

integration of the contacts can be conducted in two different ways: the integration of the metallization on n-InP and p-InGaAs can be (i) sequential or (ii) simultaneous.

A simultaneous opening of both cavities would drastically reduce the number of integration steps. In this case, a unique metallization must be integrated on both n-InP and p-InGaAs. If this solution is ultimately retained, based on the results emanating from Chapter 3 and Chapter 4, the Ni_2P combined with an in situ pre clean must be used. Indeed, the latter provides the best solution with specific contact resistivities of 4.3 x 10^{-6} Ω.cm^2 and 1.2 x 10^{-5} Ω.cm^2 respectively on n-InP and p-InGaAs right after deposition. This type of metallization also presents the advantage of being thermally stable at least up to 350 °C on both surfaces, therefore enabling the application of thermal budgets during the subsequent integration steps.

However, as already discussed in section 2.5, the n-InP and p-InGaAs surfaces are separated by several micrometers in the III-V laser laser device. Therefore, a simultaneous opening of both cavities would require the use of thick hard masks (t > 1.2 µm) and etching stop layers. While this solution is not unfeasible, one might consider a sequential opening of the cavities. In this case, the metallizations can be differentiated but one must take into account the thermal stability of the compounds in order to determine which semiconductor should be contacted first. Based on the specific contact resistivity values, and on the results presented in Chapter 3, it appears that while the Ni_2P combined with an Ar^+ preclean is the most suitable solution on n-InP, the Ni would minimize the contact resistivity to p-InGaAs surfaces. Both metallizations can be used as deposited in which case integrating the metallization on n-InP or on p-InGaAs first would not matter. One could also choose to use the as deposited Ni_2P on n-InP and to conduct a thermal treatment on the Ni/InGaAs system in order to further decrease the associated resistivity. In this case, the contact on p-InGaAs must be integrated first in order to fully optimize both contacts. This integration would give access to resistivities as low as 4.3 x 10^{-6} Ω.cm^2 and 5.6 x 10^{-6} Ω.cm^2 respectively on n-InP and p-InGaAs. In order to fully complete this study, it would be of great interest (i) to probe additional annealing temperature and durations on the relevant systems in order to further decrease the contact resistivity and (ii) to simulate the thermal budget to which the integrated metallizations are subjected during the subsequent integration steps. Metallurgical and electrical characterizations conducted after additional thermal treatments would provide an insightful indication of the integrated metallizations' thermal stabilities. Finally, integrating the contacts thanks to the innovative integration scheme presented in Chapter 2 will enable the contact resistivity to be further decreased (see results obtained on the Ti/InGaAs system annealed at 350 °C).

4.6 Impact of the dielectric stack on the contact resistivity

4.6.1 Experimental procedure

As briefly detailed previously, the second axis of the present electrical study aims to probe the impact of the dielectric encapsulation on the specific contact resistivity. Because the dielectric compounds are deposited and then etched on the III-V surfaces were the metallizations are integrated, they might modify the electrical properties of these regions. In order to study this point, classical contact stacks were used:

- Au (250 nm) / Pt (75 nm) / Ti (25 nm) on n-InP (N_D= 3.10^{18} cm^{-3}) and p-InGaAs (N_A= 3.10^{19} cm^{-3});
- Au (250 nm) / Pt (75 nm) on p-InGaAs (N_A= 3.10^{19} cm^{-3}).

The considered dielectric compounds are the ones that were presented in section 2.4, i.e., the conformal SiN deposited at 300 °C, the low stress SiN, the SiO_2 and finally the Al_2O_3. Because the integration scheme presented in Chapter 2 requires the presence of a SiN hard mask on the III-V surface, all stacks probed in this study present a SiN layer at their bottom. The resulting dielectric stacks are therefore:

- Low stress SiN (200 nm);
- Conformal SiN (200 nm);
- SiO_2 (150 nm) / conformal SiN (50 nm);
- Conformal SiN (50 nm) / Al_2O_3 (100 nm) / conformal SiN (50 nm).

The samples manufacture, which is very similar to the previous one, includes a wet surface preparation in a diluted HCl : H_2O (1 : 10). After this step, the III-V wafers are transferred in the dielectric deposition chambers were the above mentioned stacks are deposited. The contact lithography level then enables the patterning of the contact cavities thanks to a SF_6-based dry etching down to the InP or InGaAs surfaces. In order to suppress the oxides and contaminants before the integration of the metallization, the samples are once again dipped into a diluted HCl : H_2O solution and rinsed in deionized water. The classical stacks are then deposited by sputtering at a temperature lower than 100 °C and etched thanks to the metal lithography level down to the top of the dielectric stack. Finally, the III-V active epitaxy is patterned in order to confine the current streamlines thanks to the wet etchings (see details in section 4.5.1).

Additionally to these samples, reference ones were also fabricated. The latter involve a lift-off integration, and therefore do not include any dielectric compound. The procedure followed for their integration firstly includes the wet III-V surface preparation. Then, a photoresist is deposited and patterned before a new surface preparation and the deposition of the metal stacks. At this point, the resist is lifted off which results in the definition of isolated metallic pads. Finally, the III-V stacks are patterned in order to limit the current crowding.

The samples fabricated for this study are summarized in Table 4.5.

Table 4.5: Recapitulative chart of the samples fabricated for the study of the dielectric encapsulation's impact on the electrical performances of the contacts.

Active epitaxy	n-InP	X	X	X	X	X										
	p-InGaAs						X	X	X	X	X	X	X	X	X	X
Integration	Lift-off	X					X					X				
	Planar		X	X	X	X		X	X	X	X		X	X	X	X
Metallic stack	Au (250 nm) / Pt (75 nm) / Ti (25 nm)	X	X	X	X	X	X	X	X	X	X					
	Au (250 nm) / Pt (75 nm)											X	X	X	X	X
Dielectric stack	Low stress SiN (200 nm)		X					X					X			
	Conformal SiN (200 nm)			X					X					X		
	SiO_2 (150 nm) / conformal SiN (50 nm)				X					X					X	
	Conformal SiN (50 nm) / Al_2O_3 (100 nm) / conformal SiN (50 nm)					X					X					X

4.6.2 Experimental results

The data treatment procedure followed on all the samples presented in Table 4.5 corresponds to the one adapted to non-alloyed contacts. The I(V) characteristics were either non-linear, in which case the contact was declared as being Schottky, or linear in which case the corresponding specific contact resistivities were extracted. The obtained results are displayed in Figure 4.36. Note that the Au/Pt/Ti/n-InP sample presenting the low stress SiN unfortunately provided inoperable results because of important defects present in the metallization stack.

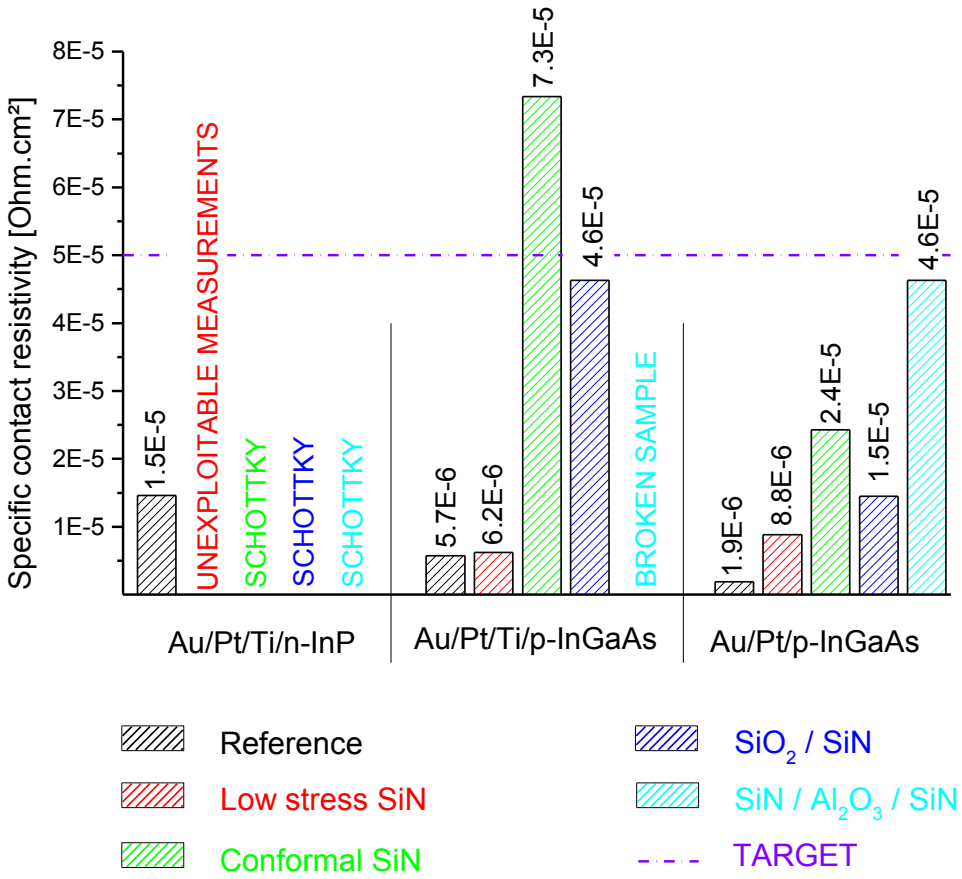


Figure 4.36: Specific contact resistivities extracted thanks to the TLM method highlighting the impact of the dielectric encapsulation on the electrical performances of the classic contacts on n-InP and p-InGaAs.

Generally speaking, and no matter the nature of the semiconductor and that of the metallization, the planar integration of the contacts leads to a degradation of their electrical performances. On n-InP, while the Au/Pt/Ti contact is ohmic when integrated thanks to a lift-off method, it constantly becomes Schottky when a dielectric stack is used. Deterioration is also observed on p-InGaAs surfaces with both metallizations. However, the latter does not change the nature of the contacts that are still ohmic but leads to an increase of the specific contact resistivities.

These deteriorations can be linked to several factors, if not to a combination of them. Contrary to the lift-off integration, the planar one involves steps that can modify the III-V surface where the contacts are integrated. Indeed, while the first kind of integration only requires the deposition and the lift-off of a resist, the second one involves the deposition of a dielectric stack along with its removal thanks to a dry etching. First of all, we saw in section 2.4 that the various dielectric compounds are deposited by PE-CVD. The latter requires the use of hydrogenated plasmas and might therefore lead to some H incorporation in the III-V compounds. Unfortunately, the presence of H in doped epitaxies can be responsible for a passivation of the doping species therefore leading to a deterioration of the

electrical performances of the contacts [45, 46]. Additionally, we demonstrated that the etching of the dielectric stack down to the III-V thanks to a SF_6-based plasma modifies both the roughness and the stoichiometry of InP and InGaAs surfaces. Therefore, this integration step having a direct impact on both the morphology and the composition of the III-V, it might as well modify the electrical properties of the contacts integrated on these surfaces. However, even if this process most likely participates to the observed modifications between the two types of integration, it does not explain the differences present between the various dielectric stacks. Indeed, as displayed in Figure 4.36, the specific contact resistivity strongly depends on the nature of the dielectric stack. Yet, the layer in contact with the III-V is consistently composed of SiN. Therefore, it is very unlikely that the observed differences are due to an interaction of this layer with the InP or InGaAs. One must therefore consider an additional intrinsic parameter varying from one dielectric stack to another and that could influence the contact resistance, *i.e.*, the stress of the various compounds (Figure 4.37).

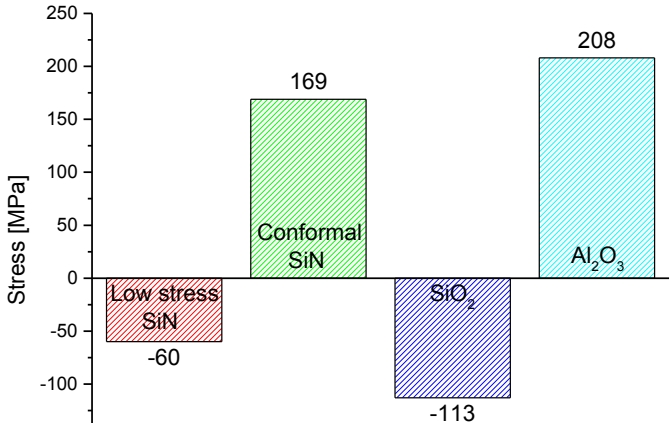


Figure 4.37: Measured stresses of the low stress SiN, conformal SiN, SiO_2 and Al_2O_3.

In first instance the direct impact of the stress on the specific contact resistivity might come as a surprise as the dielectric stack is actually opened and therefore absent in the metal / semiconductor contact regions. Yet, similar results were reported in the literature in $Al_{0.4}Ga_{0.6}As$/GaAs heterostructures contacted with Au/Ni/Au/Ge/Ni stacks [47]. Note that the following theories will be developed in the general case. The related effects strongly depend on the nature of the stress (compressive of tensile) but also on the crystalline direction over which it is applied. Unfortunately, because of the smallness of the samples, some of our TLM structures were patterned in the [100] direction while others were patterned in the [010] direction. The direction and the sign of the stress both varying from one sample to another, a direct extraction of their isolated impact is thus not possible. Nonetheless, it is clear that the stress of the dielectric overlayers impacts the contact resistance. In order to identify the physical phenomena that could be responsible for this evolution, one must consider the repartition of the stress in TLM structures. As already mentioned, the latter

are composed of cavities opened in a dielectric stack and filled with metal. Therefore, the dielectric stack is not continuous, and the discontinuities are located at the edges of the contact regions. The repartition of the stress in comparable situations was studied and reported in the literature, mostly on GaAs substrates [48-50]. It was shown that when windows are opened in dielectric stacks, the edges exert a force on the underlying semiconductor which results in the appearance of a stress field building up to high stress values beneath the edges of the dielectric. While the values reported in the literature somehow vary, most authors report the fact that the stress transmitted in the semiconductor is non-negligible in a region within six to ten layers thicknesses from the edge of the window. Note that this region might correspond to a non-negligible portion of the transfer length, *i.e.*, of the surface over which the charge carriers transit. This stress gives rise to a strain / to a distortion of the lattice, among other calculated and represented in [49] (Figure 4.38).

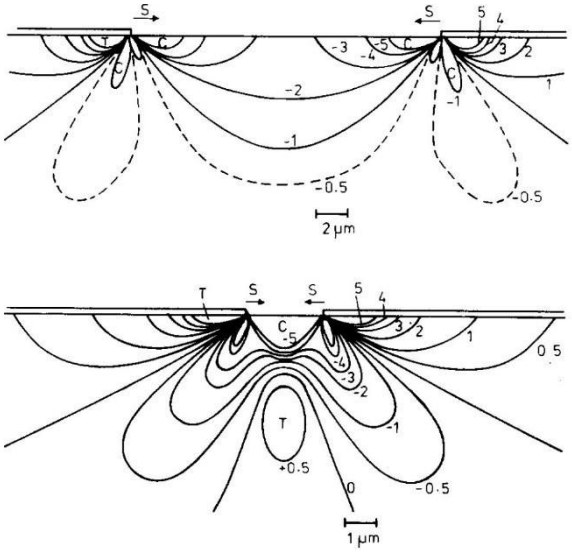


Figure 4.38: Tensile strain in GaAs beneath a 300 nm thick and (a) 20 µm wide or (b) 2.5 µm wide oxide stripes (stress between 100 and 1000 MPa). The contour lines are marked in unit of strain of 10^{-4}. Note that *T* stands for tension and *C* for compression [49].

It was demonstrated in literature that the presence of stress and strain underneath the dielectric openings leads to a modification of the electrical properties of the contacts [47]. However, the origins of these variations can be linked to several mechanisms that will be detailed in the following.

A first hypothesis that can be formulated concerns the spatial distribution of the doping species underneath the contact region. It was theorized and experimentally demonstrated that under a stress, the doping species present in a semiconductor might be redistributed [51-53]. Under the theory of dopant diffusion mediated by point defects, *i.e.* interstitial sites and vacancies, this mechanism is attributed to a variation of these point defects' concentration with the applied stress. It was shown that under positive stress (tensile), the enthalpy of formation of interstitial sites increases while that of vacancies decreases by quantities that are proportional to the applied stress.

The opposite effect was also observed under compressive stress. The stress therefore results in point defects movement which constitutes the driving force for the dopant diffusion where the point defects population is increased. Therefore, one would expect the doping species to diffuse preferentially in the stressed regions of the TLM structures, *i.e.*, at the edges of the contact cavities. However, this theory is highly questionable in our experiments as one would expect this mechanism to enhance the conduction and thus to decrease to contact resistivity. Although the absence of this phenomenon in our structures cannot be affirmed, it seems reasonable to assume that it is at least of minimal influence compared to the following mechanisms.

The application of a stress also directly impacts the band diagrams of the metal / semiconductor system. More precisely, under a stress, the band bending along with the energy-band edges change in the various valleys of the semiconductor's band diagram [54, 55]. The effective masses of the charge carriers being inversely proportional to the band bending, the application of a stress therefore modifies them. Ultimately, the way the charge carriers manage to get to and go through the barrier is impacted as it depends on these effective masses [56]. As a consequence, applying a stress on a junction (heterojunction [54], metal / semiconductor…) might modify the conduction of the majority charge carriers through the barrier and therefore the resulting contact resistivity.

Finally, the InP and InGaAs are non-Centro symmetric crystals and exhibit a piezoelectric behavior that must be considered. Several studies relate this kind of behavior as well as its impact on the electrical performances of FETS and AlGaAs/GaAs heterostructures [47, 50, 57]. In their paper, Asbeck *et al* calculated the piezoelectric charge density in GaAs located under an opened window of Si_3N_4 [57] Figure 4.39.

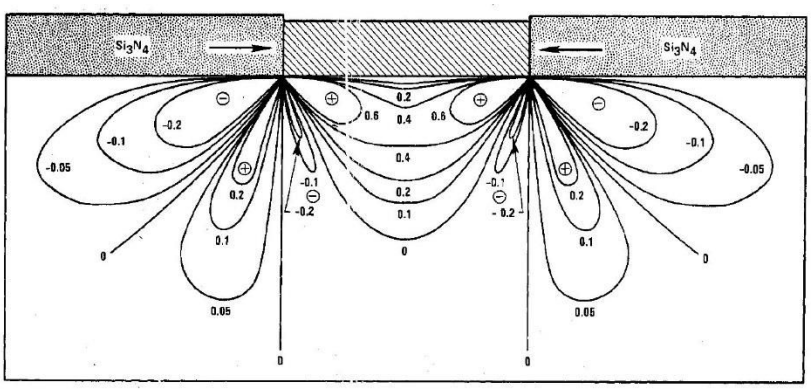


Figure 4.39: Calculated piezoelectric charges density (normalized) extracted from [57]. The dielectric layer is composed of Si_3N_4 whose stress is equal to 500 MPa. The layer is 200 nm-thick and the window is 1 µm wide [57].

These piezoelectric charge densities add up to the already established charge densities due to the doping of the semiconductor. Note that the spatial repartition of the charges strongly depends on

the orientation of the stress. If a device or a TLM structure is oriented along a direction or at 90 ° from it, the resulting densities are of identical magnitude, but of opposite sign. As a consequence, the piezoelectric effect can strongly affect and modify the electric performances of the contacts by changing the charge densities in the stressed regions. Close to the metal/semiconductor interface these regions representing a non-negligible portion of the transfer length, this effect might result in non-negligible modification of the contact resistance.

4.6.3 Conclusion on the impact of the dielectric encapsulation

The integration of the contacts on the laser structures in a silicon-compatible fab-line requires the suppression of the lift-off processes and the use of planar processes only. In chapter 2, we saw that, in order to enable such integration, a dielectric stack is deposited on the III-V surfaces and patterned to define contact cavities. In this section, we demonstrated that this planar integration has a negative impact on the specific contact resistivities which are, without exception, always degraded compared to those obtained on the lift-off references. This deterioration of electrical performance can be attributed in first instance to the modification of the III-V surface state by the dielectric deposition itself and by its subsequent dry etching. Indeed, the hydrogenated plasma used for the deposition of most dielectric compounds most likely leads to some H incorporation and thus to a decrease of the active doping species concentration. Additionally, the SF_6-based plasma used for the opening of the cavities was proven to increase the InP and InGaAs roughness and to modify their stoichiometry (see section 2.5). On top of that, while the layer in contact with the III-V is always composed of SiN deposited at 300 °C, additional variations are observed when the nature of the dielectric over-layers are modified. These modifications are imputed to the dielectric compounds' intrinsic stresses that are transmitted in the semiconductor in the contact regions. Several phenomena modifying the charge carriers repartition can indeed occur in a stressed III-V semiconductor as listed below:

- The doping species can be redistributed in the semiconductor under a stress due to a modification of the vacancies and interstitial sites concentration;
- The band diagrams can be distorted which leads to a modification of the current transport mechanisms and therefore of the electric properties of the metal / semiconductor junction;
- The stress can give rise to a piezoelectric effect and therefore to additional charge densities in the contact region.

It is important to note that the stress in the semiconductor is concentrated in a region within six to ten layers thicknesses from the edge of the dielectric window. Therefore, the maximum intensity of the above listed mechanisms occurs within a non-negligible portion of the transfer length. As a consequence, these phenomena directly impact the shape of the Schottky barrier present at the

metal / semiconductor interface and therefore the specific contact resistivity. An additional study decoupling the effects of the applied stress's nature and orientation would be of great interest to identify which dielectric stack is the most favorable, and along which crystalline direction the contacts should be integrated.

4.7 Conclusion

This chapter was dedicated to the electrical study of Ni and Ti based Si-compatible contacts. In first instance, thanks to M/SC band diagrams the origins of the contact resistance / resistivity were described. Based on the description of the various conduction mechanisms and of the associated equations, we were able to identify the levers available to decrease the contact resistance. Additionally to the doping of the semiconductor which enhances the FE and TFE conduction modes, one can tune the Schottky barrier height by changing the metallization in contact with the semiconductor (TE conduction mode). In this scope, the deposition or the formation of intermetallic compounds is of great interest as it gives access to a wide range of phases and therefore work functions, and because it allows decreasing the impact of the original semiconductor surface state.

Additionally to these theoretical considerations, we presented and reviewed one of the most classical setup used for the extraction of the specific contact resistivity, namely the TLM. Among others, we highlighted the limitations of the methods described in the literature used to account for the modification of the semiconductor sheet resistance under the contact area after thermal treatments. The latter requires the determination of the so called end resistance that can be performed thanks two different setups. Unfortunately both lead to unreliable results, mainly because of parasitic effects that cover up the actual end resistance value. Even though upgrades were proposed and implemented, an accurate determination of this parameter was not enabled in an array of contacts. As a consequence, although it might somewhat underestimate the actual contact resistivity, the classical TLM extraction was used for every sample probed in this electrical study.

The Silicon photonics requiring the formation of ohmic contacts with specific contact resistivities lower than 5×10^{-5} $\Omega.cm^2$, the first focus was placed on the determination of the most accurate Si-compatible metallization(s) on n-InP and p-InGaAs. Overall, because the integration of both contacts can be (i) simultaneous or (ii) sequential on the laser, two main options are available. (i) In the first case, the Ni_2P combined with an optimized in situ preclean provides the best compromise on both semiconductor. Indeed, the latter enables reaching specific contact resistivities of 4.3×10^{-6} $\Omega.cm^2$ and 1.2×10^{-5} $\Omega.cm^2$ respectively on n-InP and p-InGaAs right after deposition. This type of metallization additionally presents the advantage of being thermally stable at least up to 350 °C on

both surfaces, therefore enabling the application of thermal budgets during the subsequent integration steps. (ii) In the second case, both contacts can be individually optimized. From this perspective, the contact on p-InGaAs should be integrated first thanks to a Ni metallization annealed at 350 °C for 60 seconds. This annealing treatment leads to the formation of the electrically favorable $Ni_6InGaAs_2$ compound therefore decreasing the contact resistivity down to 5.6 x 10^{-6} Ω.cm^2. The contact on n-InP should be composed of Ni_2P preceded by an in situ surface preparation. This metallization provides resistivities as low as 4.3 x 10^{-6} Ω.cm^2 and presents the advantage of being stable up to 350 °C where the contact resistivity only increases up to 7.3 x 10^{-6} Ω.cm^2.

Finally, the impact of the dielectric encapsulation required for the planar integration of the contacts was probed. It was shown that, without exception, the latter tends to degrade the contact resistivity compared to lift-off based references. In first instance this contact resistivity increase is attributed to the deposition and subsequent etching of the dielectric stack. The latter was indeed proven to increase the InGaAs and InP roughness while incorporating some H and modifying their stoichiometry. Additionally, while the layer in contact with the semiconductor was always composed on SiN, variations of the electrical parameters were observed from one dielectric stack to another. These differences are attributed to the stress of these compounds that is transmitted in the semiconductor underneath the edges of the contact cavities. The latter can give rise to various phenomena that modify the conduction of the charge carriers: (i) a redistribution of the doping species can occur in the semiconductor, (ii) the band diagram and therefore the Schottky barrier can be distorted under the effect of the stress and (iii) piezoelectric charges can add up to the already present doping densities in the InP and InGaAs. Therefore, encapsulating the laser has a direct impact on the electrical performances of the integrated contacts. In order to take the most out of these mechanisms, further characterizations decoupling the nature of the stress (compressive or tensile) from the crystalline orientation over which it is applied would be of great interest.

CHAPTER 4 - Bibliographic references

[1] H. Fanet H. Mathieu. *Physique des semiconducteurs et des composants électroniques, 6eme édition*. 2009.

[2] S.M. Sze. *Physics of Semiconductor Devices*. 3rd edition, 2007.

[3] E. H. Rhoderick and R. H. Williams. *Metal-Semiconductor contacts, second edition*. Oxford Science Publications, Clarendon Press, Oxford, 1988.

[4] H.K. Henisch. *Semiconductor Contacts. An approach to ideas and Models*. Oxford Science Publications, Clarendon Press, Oxford, 1984.

[5] W. Schottky. Halbleitertheorie der sperrschicht. *Naturwissenschaften*, 26(52):843–843, 1938.

[6] N.F. Mott. Note on the contact between a metal and an insulator or semi-conductor. *Proceedings of the Cambridge Philosophical Society*, 34:568, 1938.

[7] J. Bardeen. Surface states and rectification at a metal semi-conductor contact. *Physical Review*, 71:717–727, May 1947.

[8] J. E. Rowe, S. B. Christman, and G. Margaritondo. Metal-induced surface states during schottky-barrier formation on Si, Ge, and GaAs. *Physical Review Letters*, 35:1471–1475, 1975.

[9] A. M. Cowley and S. M. Sze. Surface states and barrier height of metal-semiconductor systems. *Journal of Applied Physics*, 36(10):3212–3220, 1965.

[10] H.A. Bethe. *MIT Radiation Lab Report*, 43-12, 1942.

[11] S. Tiwari. *Compound semiconductor device physics*. Academic Press, 1992.

[12] J. F. Thiery, H. Fawaz, J. C. Pesant, N. T. Linh, and G. Salmer. Beryllium ion implantation into GaAs and pseudomorphic AlGaAs/InGaAs/GaAs heterostructure. *Journal of Electronic Materials*, 26(1):16–20, 1997.

[13] H.W Dong, Y.W Zhao, and J.M Li. Annealing and activation of silicon implanted in semi-insulating InP substrates. *Materials Science in Semiconductor Processing*, 6(4):215 – 218, 2003.

[14] A. Alian, G. Brammertz, N. Waldron, C. Merckling, G. Hellings, H.C. Lin, W.E. Wang, M. Meuris, E. Simoen, K. De Meyer, and M. Heyns. Silicon and selenium implantation and activation

in $In_{0.53}Ga_{0.47}As$ under low thermal budget conditions. *Microelectronic Engineering*, 88(2):155 – 158, 2011.

[15] G. Kerrien, T. Sarnet, D. Debarre, J. Boulmer, M. Hernandez, C. Laviron, and M.-N. Semeria. Gas immersion laser doping (GILD) for ultra-shallow junction formation. *Thin Solid Films*, 453-454:106 – 109, 2004.

[16] P. G. Carey, K. Bezjian, T. W. Sigmon, P. Gildea, and T. J. Magee. Fabrication of submicrometer MOSFET's using gas immersion laser doping (GILD). *IEEE Electron Device Letters*, 7(7):440–442, Jul 1986.

[17] E. Bustarret, C. Marcenat, P. Achatz, J. Kacmarcik, F. Levy, A. Huxley, L. Ortega, E. Bourgeois, X. Blase, D. Debarre, and J. Boulmer. Superconductivity in doped cubic silicon. *Nature*, 444(7118):465–468, Nov 2006.

[18] H. Berger. Contact resistance on diffused resistors. In *IEEE International Solid-State Circuits Conference. Digest of Technical Papers. 1969*, volume XII, pages 160–161, 1969.

[19] H. Murrmann and D. Widmann. Current crowding on metal contacts to planar devices. *IEEE Transactions on Electron Devices*, 16(12):1022–1024, Dec 1969.

[20] H. H. Berger. Contact resistance and contact resistivity. *Journal of The Electrochemical Society*, 119(4):507, 1972.

[21] S.S. Cohen. Contact resistance and methods for its determination. *Thin Solid Films*, 104(3-4):361–379, June 1983.

[22] H.H. Berger. Models for contacts to planar devices. *Solid-State Electronics*, 15(2):145 – 158, 1972.

[23] W. Shockley, A. Goetzberger, and R. M. Scarlett. Research and investigation of inverse epitaxial UHF power transistors. *Research and investigation of inverse epitaxial UHF Power Transistors, Air Force Atomic Laboratory*, Tech. Report No. AL TDR 64-207, 1964.

[24] G.K. Reeves and H.B. Harrison. Obtaining the specific contact resistance from transmission line model measurements. *Electron Device Letters, IEEE*, 3(5):111–113, 1982.

[25] Ivan A. Smirnov and Sergey V. Kalinin. Analysis of certain methods for determining contact resistivity. pages 162–164, 2011.

[26] I. Ohdomari, K. N. Tu, K. Suguro, M. Akiyama, I. Kimura, and K. Yoneda. Low-temperature redistribution of As in Si during Pd_2Si formation. *Applied Physics Letters*, 38(12):1015–1017, 1981.

[27] I. Ohdomari, M. Akiyama, T. Maeda, M. Hori, C. Takebayashi, A. Ogura, T. Chikyo, I. Kimura, K. Yoneda, and K. N. Tu. Low-temperature redistribution of As in Si during Ni silicide formation. *Journal of Applied Physics*, 56(10):2725–2728, 1984.

[28] Jun Amano, P. Merchant, T. R. Cass, J. N. Miller, and Tim Koch. Dopant redistribution during titanium silicide formation. *Journal of Applied Physics*, 59(8):2689–2693, 1986.

[29] G.K Reeves and H.B Harrison. A tri-layer transmission line model applied to alloyed ohmic contacts. *Solid-State Electronics*, 38(5):1115 – 1117, 1995.

[30] G.K. Reeves, P.W. Leech, and H.B. Harrison. Understanding the sheet resistance parameter of alloyed ohmic contacts using a transmission line model. *Solid-State Electronics*, 38(4):745 – 751, 1995.

[31] G.K. Reeves and H.B. Harrison. Using TLM principles to determine MOSFET contact and parasitic resistance. *Solid-State Electronics*, 41(8):1067 – 1074, 1997.

[32] E. Dubois and G. Larrieu. Measurement of low Schottky barrier heights applied to metallic source/drain metal/oxide semiconductor field effect transistors. *Journal of Applied Physics*, 96(1):729–737, 2004.

[33] A. Appelbaum, P. M. Thomas, and P. A. Barnes. Interaction of nickel with lnP as a fonction of annealing time and temperature. *Semiconductor - based heterostructures: Interfacila structure and stability*, page 409, 1986.

[34] N.S. Fatemi and V.G. Weizer. The structural and electrical properties of low-resistance Ni contacts to InP. *Journal of Applied Physics*, 73(1):289, 1993.

[35] A. Appelbaum, M. Robbins, and F. Schrey. Sputtered Ni-P as an ohmic contact to n-InP, p-InGaAs and as a diffusion barrier. *IEEE Trans. on Electron Devices*, ED-34(5), May 1987.

[36] G.K. Reeves. Specific contact resistance using a circular transmission line model. *Solid-State Electronics*, 23(5):487 – 490, 1980.

[37] Dev Alok, B.J. Baliga, and P.K. McLarty. Low contact resistivity ohmic contacts to 6H-silicon carbide. *International Electron Devices Meeting, IEDM '93. Technical Digest.*, 1993.

[38] C. Xu, J. Wang, M. Wang, H. Jin, Y. Hao, and C.P. Wen. Reeves's circular transmission line model and its scope of application to extract specific contact resistance. *Solid-State Electronics*, 50(5):843 – 847, 2006.

[39] J. Kriz, K. Gottfried, C. Kaufmann, and T. Gesner. Determination of ohmic contacts to n-type 6H- and polycrystalline 3C-SiC using circular transmission line structures. *Diamond and Related Materials*, 7(1):77 – 80, 1998.

[40] D. Connelly, C. Faulkner, D. E. Grupp, and J. S. Harris. A new route to zero-barrier metal source/drain MOSFETs. *IEEE Transactions on Nanotechnology*, 3(1):98–104, March 2004.

[41] H. Yu, M. Schaekers, T. Schram, E. Rosseel, K. Martens, S. Demuynck, N. Horiguchi, K. Barla, N. Collaert, K. De Meyer, and A. Thean. Multiring circular transmission line model for ultralow contact resistivity extraction. *IEEE Electron Device Letters*, 36(6):600–602, June 2015.

[42] Ivana, J. Pan, Z. Zhang, X. Zhang, H. Guo, X. Gong, and Y.-C. Yeo. Photoelectron spectroscopy study of band alignment at interface between Ni-InGaAs and $In_{0.53}Ga_{0.47}As$. *Applied Physics Letters*, 99(1):012105, 2011.

[43] X. Zhang, H. Guo, X. Gong, Q. Zhou, Y.-R. Lin, H.-Y. Lin, C.-H. Ko, C. H. Wann, and Y.-C. Yeo. $In_{0.7}Ga_{0.3}As$ channel n-MOSFET with self-aligned Ni-InGaAs source and drain. *Electrochemical and Solid-State Letters*, 14(2):H60, 2011.

[44] X. Zhang, Ivana, H. X. Guo, X. Gong, Q. Zhou, and Y.-C. Yeo. A self-aligned Ni-InGaAs contact technology for InGaAs channel n-MOSFETs. *Journal of The Electrochemical Society*, 159(5):H511, 2012.

[45] B. Theys, A. Jalil, J. Chevallier, A.M. Huber, C. Grattepain, P. Hirtz, and B. Pajot. Hydrogen neutralization of dopant in p-type $In_{0.53}Ga_{0.47}As$. *Physica B: Condensed Matter*, 170(1):421 – 425, 1991.

[46] C. Carmody, H. H. Tan, and C. Jagadish. Electrical isolation of n- and p-$In_{0.53}Ga_{0.47}As$ epilayers using ion irradiation. *Journal of Applied Physics*, 94(10):6616–6620, 2003.

[47] A. K. Fung, J. D. Albrecht, M. I. Nathan, P. P. Ruden, and H. Shtrikman. In-plane uniaxial stress effects of AlGaAs/GaAs modulation doped heterostructures characterized by the transmission line method. *Journal of Applied Physics*, 84(7):3741–3746, 1998.

[48] H. Booyens, G. R. Proto, and J. H. Basson. Strain effects associated with SiO layers evaporated onto GaAs. *Journal of Applied Physics*, 54(10):5779–5784, 1983.

[49] P. A. Kirkby, P. R. Selway, and L. D. Westbrook. Photoelastic waveguides and their effect on stripe-geometry GaAs/$Ga_{1-x}Al_xAs$ lasers. *Journal of Applied Physics*, 50(7):4567–4579, 1979.

[50] J. C. Ramirez, P. J. McNally, L. S. Cooper, J. J. Rosenberg, L. B. Freund, and T. N. Jackson. Development and experimental verification of a two-dimensional numerical model of piezoelectrically induced threshold voltage shifts in GaAs MESFETs. *IEEE Transactions on Electron Devices*, 35(8):1232–1240, Aug 1988.

[51] H. Park, K.S. Jones, J.A. Slinkman, and M.E. Law. Effects of hydrostatic pressure on dopant diffusion in silicon. *Journal of Applied Physics*, 78(6):3664–3670, 1995.

[52] M.J. Aziz. Stress effects on defects and dopant diffusion in Si. *Materials Science in Semiconductor Processing*, 4(5):397 – 403, 2001.

[53] M.J. Aziz. Dopant diffusion under pressure and stress. *Proceedings of the IEEE International Conference on Simulation of Semiconductor Processes and Devices SISPAD 2003*, pages 137–142, 2003.

[54] S. S. Lu, K. R. Lee, K. H. Lee, M. I. Nathan, M. Heiblum, and S. L. Wright. Theoretical and experimental study of the longitudinal uniaxial stress dependence of I/V characteristics in GaAs-$Al_xGa_{1-x}As$-GaAs heterojunction barriers. *Journal of Applied Physics*, 67(10):6360–6367, 1990.

[55] N. Lu, H. Guo, L. Li, J. Dai, L. Wang, W-N. Mei, X. Wu, and X.C. Zeng. Mos_2/MX_2 heterobilayers: bandgap engineering via tensile strain or external electrical field. *Nanoscale*, 6:2879–2886, 2014.

[56] C.R. Crowell. Richardson constant and tunneling effective mass for thermionic and thermionic-field emission in schottky barrier diodes. *Solid-State Electronics*, 12(1):55 – 59, 1969.

[57] P. M. Asbeck, C.-P. Lee, and M.-C. Chang. Piezoelectric effects in GaAs FET's and their role in orientation-dependent device characteristics. *IEEE Transactions on Electron Devices*, 31:1377–1380, October 1984.

GENERAL CONCLUSION

Because our needs in terms of data exchange never stopped rising over the past decades, a switch from electronical towards optical devices and interconnections was initiated. In order to miniaturize these optoelectronic devices, to optimize their performances and to minimize their fabrication cost, the III-V laser source must be directly integrated onto the 200 mm Si photonics circuit. However, up to now these 200 mm wafers were brought back to 100 mm wafers in order to be processed in III-V dedicated clean rooms once the III-V laser was bonded. The great loss generated by this kind of solution lead STMicroelectronics and the CEA-LETI to develop a new scheme enabling the processing of the wafers in 200 mm Si-compatible clean rooms even after the III-V laser bonding. In order to enable this integration, one of the keys lies in the development of Si-compatible contacts on n-InP and p-InGaAs which are necessary to electrically pump the III-V laser. In order to appropriately fulfill this function, the contacts must additionally be ohmic and present specific contact resistivities lower than 5×10^{-5} $\Omega.cm^2$.

The studies conducted in the frame of this Ph.D thesis consisted in developing a fully Si-compatible integration scheme for the contacts on p-InGaAs and n-InP. To do so, the processes traditionally used on Si surfaces were probed on III-V surfaces and adapted to them. A particular attention was also paid to the optical properties of the materials which would be situated close to the active region of the laser in order not to generate photon losses. More precisely, the integration scheme that was developed firstly requires the direct bonding of the III-V stack onto the 200 mm Silicon Photonics wafer. The T-shaped laser is then patterned into this stack thanks to a SiN hard mask whose nature must be carefully chosen in order not to degrade the III-V surfaces. Thanks to AFM measurements we were able to show that its deposition temperature must not exceed 300 °C and that, while the conformal SiN deposited by PE-CVD at 300 °C constitutes a first appropriate solution, the low stress SiN would further improve the protection of the InP and InGaAs surfaces. Thanks to electrical characterizations conducted on the integrated contacts, it was shown that the latter additionally lowers the specific contact resistivity compared to the conformal SiN. In order to perform a planar integration of the contacts, a damascene approach was then selected. The latter requires a dielectric encapsulation of the laser which will be contiguous to the active region. This encapsulation must therefore enable a proper evacuation of the heat produced by the operating laser and must not generate optical losses at the emitting wavelength of the laser (λ = 1.3 – 1.55 µm) while being compatible with CMP processes. Taking into account these requirements, the low stress SiN along with the SiO_2 were selected as the most appropriate candidates for this encapsulation. The

subsequent contact cavities opening is achieved thanks to a dry etching and requires the use of a top SiN hard mask. While the etching of the top SiN and SiO_2 are not problematical, the etching of the bottom SiN is very delicate as it must not increase the semiconductor surfaces roughness, alter their stoichiometry or leave any residues. In order to fulfill the entirety of these requirements, the bottom SiN layer must be etched thanks to a combination of two steps. The first one consists in partially etching the SiN thanks to a CH_2F_2-based dry process. Then, in order to preserve the InP and InGaAs surfaces and to remove potential residues, the last SiN nanometers must be removed thanks to a wet etching, for example composed of diluted hydrofluoric acid. Before integrating the contact metallization, a proper surface preparation must be conducted in order to remove any contaminants and oxides. A scheme combining diluted or concentrated HCl and Ar^+ or He plasma treatment is well adapted for the preparation of InGaAs surfaces while the preparation of InP surfaces is more delicate and requires the use of diluted HCl combined with an He plasma treatment. Once the surfaces are clean, two strategies can be followed to integrate the contact metallization: (i) One can choose to deposit directly the metal(s) or the intermetallic compound(s) of interest on the III-V surface. The stabilization of the phase(s) is achieved by mean of an annealing process. (ii) One can also choose to deposit a metal and to perform a thermal treatment for the purpose of forming one or several intermetallic compound(s) at the interface by solid state reaction with the III-V. Thanks to electrical characterizations, we showed that performing a thermal treatment is of great interest when the surfaces cannot undergo in situ plasma treatments as it allows decreasing the impact of the thin oxides layers that can be present on the semiconductor surface. Anyway, the integration of the contacts on the laser can be (i) simultaneous or (ii) sequential because of the important topography existing between the n-InP and p-InGaAs surfaces on the laser. (i) In the first case, the Ni_2P combined with an optimized in situ preclean provides the best compromise on both semiconductors. Indeed, the latter enables reaching specific contact resistivities of 4.3×10^{-6} $\Omega.cm^2$ and 1.2×10^{-5} $\Omega.cm^2$ respectively on n-InP and p-InGaAs right after deposition. This type of metallization additionally presents the advantage of being thermally stable at least up to 350 °C on both surfaces, therefore enabling the application of thermal budgets during the subsequent integration steps. (ii) In the second case, both contacts can be individually optimized. From this perspective, the contact on p-InGaAs should be integrated first thanks to a Ni metallization annealed at 350 °C for 60 seconds. This annealing treatment leads to the formation of the electrically favorable $Ni_6InGaAs_2$ compound therefore decreasing the contact resistivity down to 5.6×10^{-6} $\Omega.cm^2$. The contact on n-InP should be composed of Ni_2P preceded by an in situ surface preparation. This metallization provides resistivities as low as 4.3×10^{-6} $\Omega.cm^2$ and presents the advantage of being stable up to 350 °C where the contact resistivity only increases up to 7.3×10^{-6} $\Omega.cm^2$. In order to electrically connect the metallizations that are located at the bottom of the contact cavities, plugs are finally integrated. Here again, their planar integration is achieved thanks to a damascene approach requiring a new dielectric encapsulation. To enable the subsequent plugs polishing, cavities that are about 5 to 10 µm wide are opened in this

encapsulation thanks to a dry etching. The plugs are then composed of a F-diffusion barrier that also acts as a nucleation layer for the filling metal which is composed of W. The liner can be composed of CVD-deposited Ti/TiN but an innovative solution consisting in depositing a F-less W is being developed. It appears that the F-less W resistivity is at least two times less important than that of the classical TiN liner which opens the way for lowering the plug resistivity and therefore to a minimization of the overall resistance.

In this Ph.D thesis, a first generation of Si-compatible contacts was therefore developed on n-InP and p-InGaAs surfaces. The results obtained being in accordance with the specifications of the Silicon Photonics, these contacts will soon be integrated onto actual laser devices. However, these studies also underlined the impact of each and every one processing step on the morphological and electrical characteristics of the contacts. It was for example shown that the specific contact resistivity obtained on the Ti/p-InGaAs system integrated thanks to the fully Si-compatible integration (TASP) is almost one order of magnitude lower than the one obtained on same contact integrated thanks to the simplified integration (MELT). It is also important to note that some of the recommendations that were given throughout this Ph.D thesis could not always be implemented in the Si-compatible integration scheme because of their unavailability during the processing of the wafers. Some of them are however now available, such as the low stress SiN, and will enable a substantial improvement of the electrical and morphological properties of the contacts. In order to go even further in this optimization, it would be of great interest to probe the impact of the dry etching and of the various surface preparations on the electrical properties of the contacts. Because some surface preparations modify the stoichiometry of InP surfaces, they might have a non negligible impact on the phase sequences and therefore on the electrical properties of the contacts. Additionally, the metallization in contact with the n-InP and p-InGaAs being determining, testing additional thermal treatment temperatures and durations would also be very relevant. In the case of intermetallic compounds' formation, once the nature of the metallization is fixed, it will be of great interest to develop selective etchings in order to remove the metal that did not react. Finally, some effects such as the link between the nature of the dielectric encapsulation and the specific contact resistivity would be worth further investigating in order to extensively identify the mechanisms responsible for the observed variations.

APPENDIX

A1 Determination of the Transmittance, Reflectance and Absorbance of the dielectric compounds [Chapter 2]

A2 Determination of the refractive index of the dielectric compounds [Chapter 2]

A3 Metallurgical study of the Ti/InGaAs system: determination of the phase sequence [Chapter 3]

A4. Current transport mechanisms in a M/SC system [Chapter 4]

A5 Transmission Line Model (TLM) and specific contact resistivity extraction [Chapter 4]

A1. Determination of the Transmittance, Reflectance and Absorbance of the dielectric compounds [Chapter 2]

The transmittance (T), reflectance (R) and absorbance (A) of the selected dielectrics compounds were measured thanks to a classical setup schematized in Figure A1. 1. An incident beam (I_0) is sent on a silicon wafer on which a dielectric layer is deposited. When it encounters the wafer, this beam is split up into two components, the transmitted (I_T) and the reflected (I_R) beams that are collected by two detectors. The maximization of the dielectric layer's thickness is essential as it allows decreasing the uncertainty of measurement. The calculations of the T, R and A coefficients are made thanks to Equation A1. 1 to Equation A1. 3.

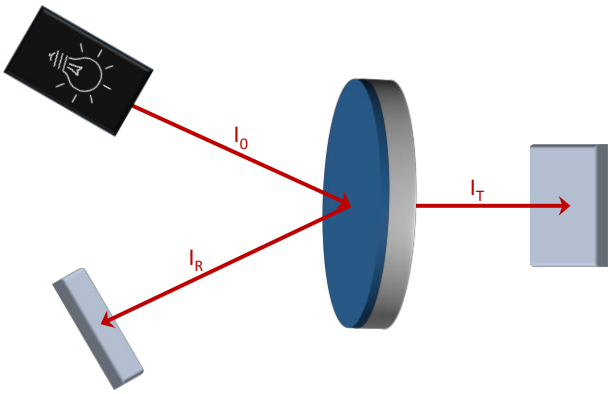


Figure A1. 1: Optical setup used for the measurement of R and T parameters of low stress SiN, conformal SiN, SiO_2 and Al_2O_3 @ 0.8 – 1.6 µm.

$$T = \frac{I_T}{I_0}.100\ [\%]$$ **Equation A1. 1**

$$R = \frac{I_R}{I_0}.100\ [\%]$$ **Equation A1. 2**

$$A = 100 - T - R\ [\%]$$ **Equation A1. 3**

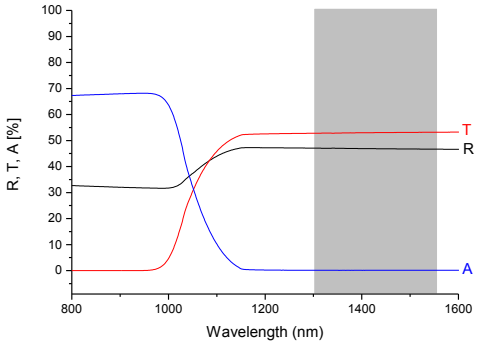
The chosen incident beam wavelengths range from 0.8 µm to 1.6 µm to cover properly the wavelength range of interest, *i.e.* 1.3 to 1.55 µm. Generally speaking, the Si substrate which is 725 µm thick might account for a non-negligible part of the absorption phenomenon that is ruled as following:

- For $E < E_{GAP}$, or $\lambda > \lambda_{GAP}$, the absorption does not occur;
- For $E > E_{GAP}$, or $\lambda < \lambda_{GAP}$, the absorption occurs and its intensity is a function of the wavelength.

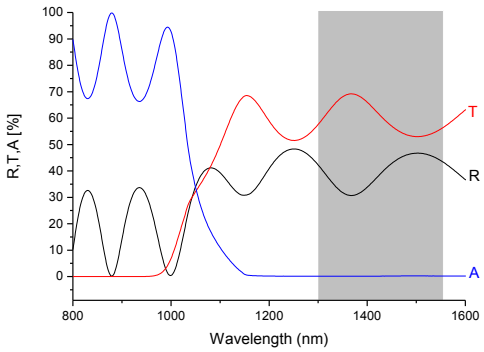
As a result, Si, which bandgap energy is equal to 1.1 eV (λ_{GAP} = 1.13 µm) will strongly absorb from 0.8 µm to 1.13 µm and will be transparent for higher wavelengths. Its contribution is complex as the various interfaces significantly influence the global result by modifying the reflection coefficient. Therefore, all measurements were performed with the same substrates in order not to induce any variability. Similarly, comparing the performed R, T and A measurements with the literature does not seem appropriate.

The three parameters are plotted as a function of the wavelength for the reference Si wafer and for the four dielectric compounds in Figure A1. 2.

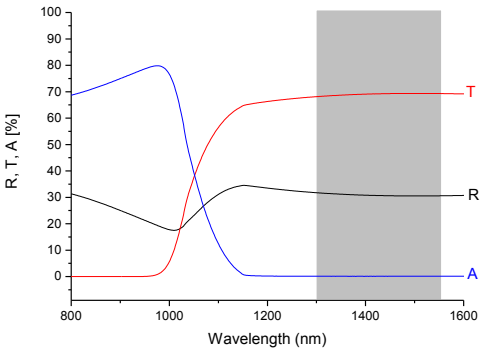
Si reference



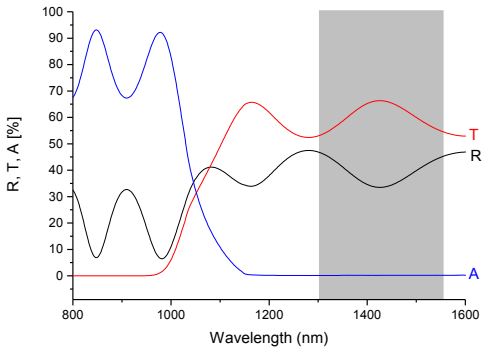
Low stress SiN / Si



Conformal SiN / Si



SiO_2 / Si



Al_2O_3 / Si

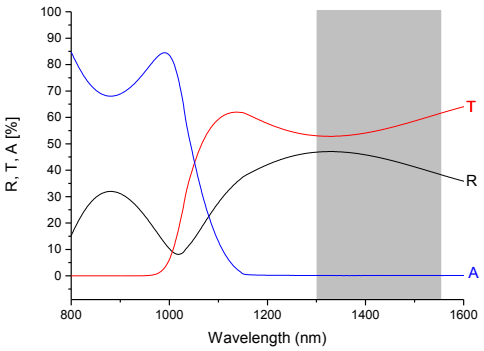


Figure A1. 2: Measured R and T and calculated A coefficients @ 0.8 – 1.6 µm for reference Si, low stress SiN, conformal SiN, SiO_2 and Al_2O_3.

One can notice that the absorption coefficient of all stacks is high for wavelengths ranging from 0.8 µm to approximately 1.1 µm, and sharply decreases afterwards. As we explained before, the

band gap wavelength of Si being of 1.13 µm, it is absorbent for $\lambda < 1.13$ µm. Therefore, the calculated A coefficient is almost completely due to the presence of Si in the stack for this range of wavelengths. On can also observe the presence of fringes that are generated by interferences that occur in the dielectric compounds, and that are therefore absent in the Si reference wafer. These interferences can be constructive or destructive which leads to an oscillation of the R, T and A values as a function of the wavelength. For example, considering the SiO_2 sample leads to the following observations:

- The transmission minimum of the SiO_2/Si system corresponds to that of Si
- The reflection maximum of the SiO_2/Si system corresponds to that of Si

In other words, adding a SiO_2 layer on top of a Si substrate will, counter-intuitively, increase the transmission (T) of the global system. This phenomena is directly linked to the modification of the interfaces, and more precisely to the suppression of the air/Si interface where an important reflection occurs (high R coefficient).

A2. Determination of the refractive index of the dielectric compounds [Chapter 2]

In order to measure the refractive indexes of the four dielectric compounds, a spectroscopic ellipsometry characterization was performed on the stacks described in Table 2.4 [1, 2].

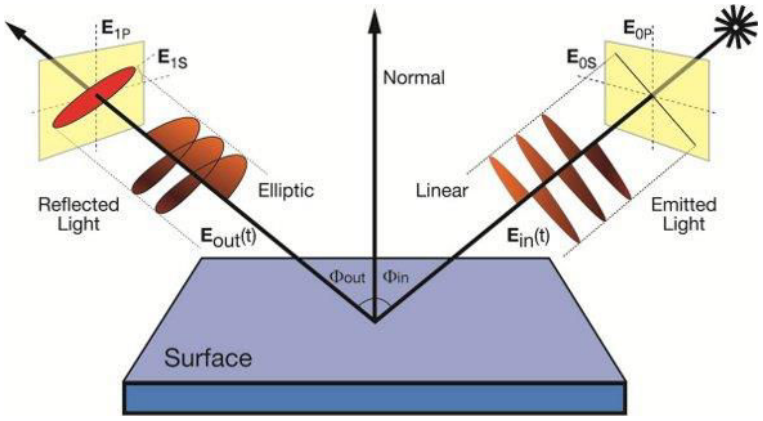


Figure A2. 1: Schematic representation of a spectroscopic ellipsometry setup used for the determination of the refractive indexes of low stress SiN, conformal SiN, SiO_2 and Al_2O_3 @1.3 – 1.55 µm [3].

As schematized in Figure A2. 1, a linearly polarized light is sent on the wafer. Part of it is transmitted through the sample while another part is reflected. The electric field of the incident (i), refracted (t) and reflected (r) beams can be described as the sum of two contributions: a polarization parallel to the incidence plane, noted E_{xp}, and an orthogonal polarization, noted E_{xs}. The complex coefficients corresponding the reflection, r_p and r_s, are calculated as follows:

$$r_p = \frac{E_{rp}}{E_{ip}} = |r_p|.e^{j\delta_p}$$ **Equation A2. 1**

$$r_s = \frac{E_{rs}}{E_{is}} = |r_s|.e^{j\delta_s}$$ **Equation A2. 2**

With $|r_p|$ and $|r_s|$ the modulus and δ_p and δ_s the phases of r_p and r_s.

When it interacts with the sample, the beam polarization changes to become elliptic. The ellipsometry consists in characterizing this ellipse thanks to the ratio ρ:

$$\rho = \frac{r_p}{r_s} = \left|\frac{r_p}{r_s}\right|.e^{j(\delta_p - \delta_s)}$$ **Equation A2. 3**

$$\text{Also noted } \rho = \tan(\psi) \,.\, e^{j\Delta}$$

Where ψ and Δ are the ellipsometric angles and are the measured parameters in an ellipsometry characterization. While they can give access to the optical characteristics of the samples an additional step of regression is compulsory. The experimental results are compared to theoretical models allowing the determination of the complex refractive index of the compound and of layer(s) thickness(es). In the case of absorbent dielectric compounds, the Tauc-Lorentz model is used [4]. An example of measurement and fit of the angles ψ and Δ is presented in Figure A2. 2 for one incident angle (65°). It is to note that three different incident angles are always probed in order to suppress the errors linked to potential correlations between the variables during the regression step.

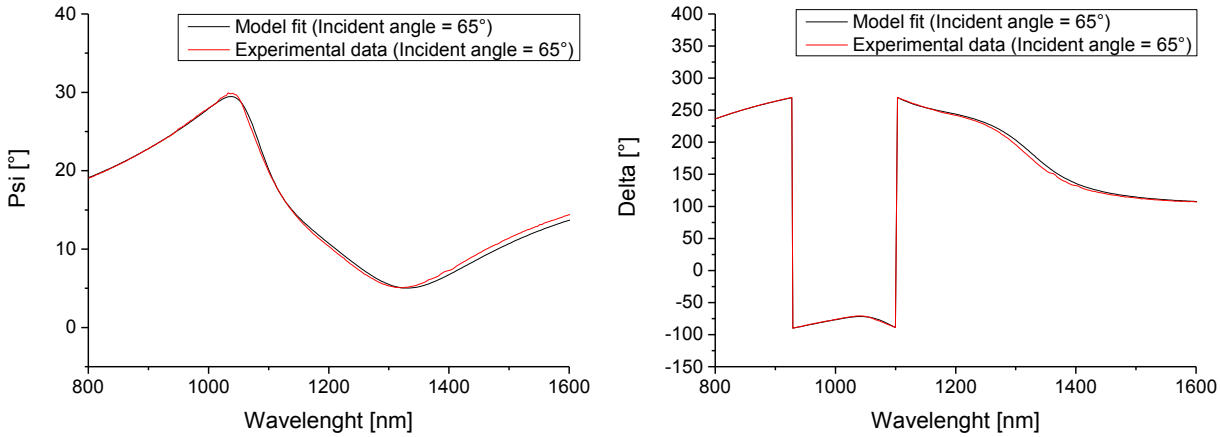


Figure A2. 2: Experimental data and corresponding fits using the Tauc-Lorentz model of ψ and Δ angles.

While the combination of an ellipsometry measurement with the Tauc-Lorentz model gives good results, it presents 2 limitations:

- Generally speaking, the ellipsometry is not sensitive to low k values (< 10^5 cm^{-1}) [5];
- In the Tauc-Lorentz model, k is equal to zero for energies lower than the band gap meaning that the intra-band absorptions are not taken into account.

In our systems, the measured absorption coefficient are always lower than the critical value, *i.e.* 3000 cm^{-1} (see Figure 2.9). Moreover, the incident wavelengths used for the measurements range from 800 nm to 1.6 µm which corresponds to energies of 0.77 eV to 1.55 eV, while the band gaps of SiN, Al_2O_3 and SiO_2 reported in the literature ranging from 2.6 to 9.3 eV [6, 7, 8]. As a consequence, the k values cannot be determined thanks to the ellipsometry technique and only the measurements of the real refractive index are presented in section 2.5.2. The absorption coefficients are thus only determined thanks to the R, T, A characterization presented in Appendix A1.

A3. Metallurgical study of the Ti/InGaAs system: determination of the phase sequence [Chapter 3]

The Ti/InGaAs system was studied by means of XRD characterization, therefore allowing the identification of the phase sequence. Similarly to all systems studied in Chapter 3, the metallurgical studies were carried out dedicated blanket samples. The latter are composed of 2 inches semi-insulating (001) InP substrates on top of which a 300 nm thick InGaAs epitaxial layer was grown. All substrates were dipped into HCl solutions (HCl : H_2O = 1 : 2) and exposed to a direct Ar^+ plasma etching in the deposition tool prior to the metal deposition process. The 20 nm thick Ti films were deposited by DC Ar sputtering respectively at 100 °C and were capped by a 7 nm thick TiN film deposited at the same temperature. Some samples were kept as deposited while some other underwent annealing treatments in order to form intermetallic compounds at the interface between the metal and the III-V semiconductor. These thermal treatments consisted in a rapid thermal annealing (RTA) under N_2 ambient for 60 seconds at temperatures ranging from 250 °C to 550 °C. All Ti/InGaAs samples were finally characterized by XRD detexturation, therefore allowing the identification of the phase sequence. The corresponding patterns are presented in Figure A3. 1.

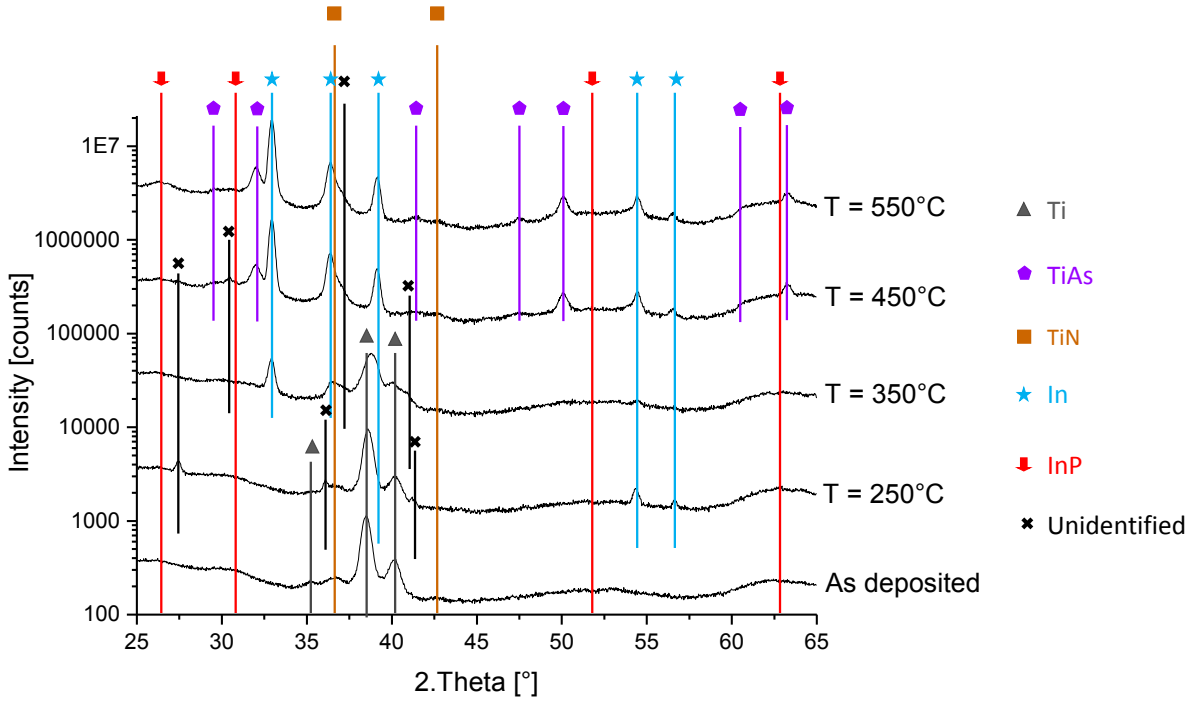


Figure A3. 1: XRD detexturation patterns of the TiN (7 nm)/Ti (20 nm)/InGaAs samples as deposited and annealed at 250 °C, 350 °C, 450 °C and 550 °C for 60 seconds (RTP). A 2° offset on the incident beam was applied in order to minimize the substrate contribution.

The characterization suggests the fact that no reaction was initiated during the deposition of the metallic layers as only the Ni and TiN diffract. However, at 250 °C and 350 °C the additional

appearance of In peaks indicates that a reaction took place. Unfortunately, several peaks (27.4 °, 36.1 °, 40.8 °) could not be indexed as no referenced compound would match their diffracting positions. Therefore, although the decrease of the Ti peaks' intensity along with the appearance of In peaks highlight a reaction, we were not able to identify the formed compounds. However, increasing again the temperature up to 450 °C and 550 °C lead to the complete consumption of the Ti and to the formation of the binary TiAs phase. In order to conserve the overall stoichiometry, this reaction is associated with some In release which strongly diffracts at this temperature. Similarly to the Ni/InP and Ti/InP systems, the In probably underwent a fusion / solidification process or a precipitation process leading to the formation of the In phase. One would expect to see a similar behaviour of the Ga but no diffraction peak could be attributed to this phase. Several hypothesis could explain the absence of Ga peaks on the diffractogram: (i) the Ga can be amorphous and (ii) the Ga can be distributed in the TiAs lattice (iii) the Ga can have crystallized under the form of nano-grains. The phase sequence observed thanks to the XRD characterization on the Ti/InGaAs system is schematically summarized in Figure A3. 2.

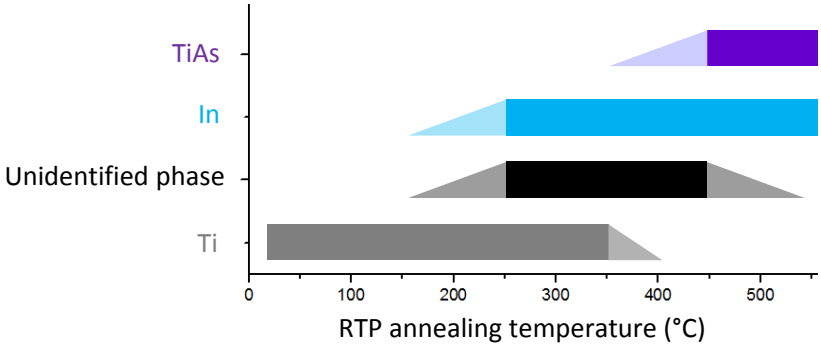


Figure A3. 2: Recapitulative chart of the phase sequence observed by XRD on the Ti/InGaAs system from deposition to RTA at 550 °C. The light fillings correspond to temperatures that were not investigated and for which only trends on the phases' evolution are displayed.

A4. Current transport mechanisms in a M/SC system [Chapter 4]

The presence of a barrier in M/SC systems results in the existence of various conduction modes that mainly rely on the majority carriers. In the following we will detail these processes based on a contact between a metal and an n-doped semiconductor. These processes are:

1. The thermionic emission (TE) which corresponds to the transport of electrons from the semiconductor to the metal, and vice versa, above the barrier;
2. The diffusion of electron from the bulk semiconductor to the space charge region;
3. The field emission (FE and TFE) which corresponds to the tunneling of the electrons through the barrier;
4. The recombination of electron / hole pairs in the space charge region;
5. The recombination of the electron / hole pairs in the neutral region, corresponding to a diffusion of the holes from the metal in the semiconductor (hole injection).

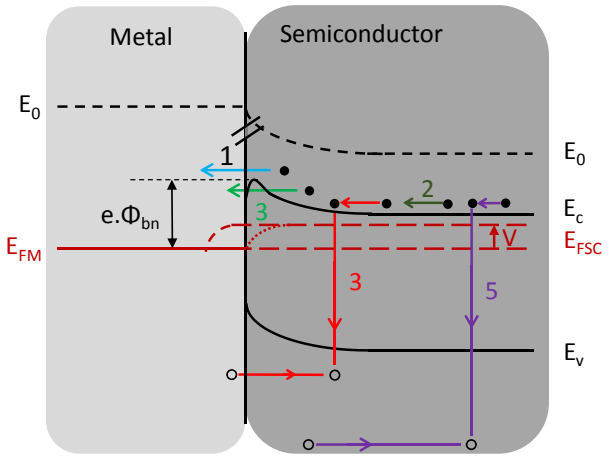


Figure A4. 1: Schematic representation of the five current transport mechanisms across a M/n-SC junction under forward bias. The quasi-Fermi level is represented according to TE theory (dashed fermi level) and diffusion theory (dotted fermi level). Note that the bias is applied on the semiconductor, the reference being the position of the metal Fermi level derived from the metal work function, Φ_m.

Emission over the barrier

The transit of electrons above the Schottky barrier can be realized thanks to two different mechanisms, which are actually the two limit cases of this phenomenon. In the case of high mobility semiconductors, the transport can be described by the thermionic emission while the dominant mechanism for low mobility semiconductors is the diffusion. Practically these two phenomena are combined and the true conduction behavior lies somewhere in between these extrema.

Thermionic emission (TE)

The thermionic emission was firstly theorized by Bethe and is valid under the following assumptions [9, 10, 11]:

- The Schottky barrier height $e.\phi_{bn}$ must be larger than kT, where k is the Boltzmann constant and T the absolute temperature (kT = 26meV @ 300 K);
- The thermal equilibrium is established at the plane that determines emission;
- The existence of a net current flow does not affect this equilibrium: the two current fluxes, one coming from the semiconductor, the other from the metal, can be superimposed;
- The current limiting process is the actual transfer of electrons across the interface between the semiconductor and the metal;
- The width of the region over which a kT drop in potential energy occurs at the barrier must be smaller than the electron mean free path.

Once these assumptions are verified, the shape of the barrier is unimportant; the current flux only depends on its height. Therefore, if the thermal energy is important enough, it will enable the transit of electrons above the barrier. When the thermal equilibrium is reached, the electron flux from the semiconductor to the metal exactly compensates that from the metal to the semiconductor. The resulting current density (J) across the barrier is equal to zero. The forward polarization ($V_F > 0$) of the contact results in an upward shift of the semiconductor's Fermi level of magnitude $e.V_F$. As a result, the barrier height seen by the electrons flowing from the semiconductor to the metal is lowered by the same quantity and the current density in forward direction (SC → M) is larger than it is in reverse direction (M → SC). A reverse polarization ($V_R < 0$) lowers the semiconductor Fermi level which results in a displacement of the charge carriers from metal to semiconductor. These situations are schematically represented in Figure A4. 2.

The current density from the semiconductor to the metal $J_{SC \rightarrow M}$ is given by:

$$J_{SC \rightarrow M} = A^* T^2 \exp\left(-\frac{e.\phi_{bn}}{kT}\right) \exp\left(\frac{eV_F}{kT}\right) \qquad \textbf{Equation A4. 1}$$

Where A^* is the effective Richardson constant for thermionic emission defined as:

$$A^* = \frac{4.\pi.e.m^*.k^2}{h^3} \qquad \textbf{Equation A4. 2}$$

The corresponding flux from the metal to the semiconductor is given by:

$$J_{M\to SC} = -A^{*}T^{2}\exp\left(-\frac{e.\phi_{bn}}{kT}\right)$$ **Equation A4. 3**

As a consequence, the net current density is:

$$J_n = J_{SC\to M} + J_{M\to SC} = \left[A^{*}T^{2}\exp\left(-\frac{e.\phi_{bn}}{kT}\right)\right]\left[\exp\left(\frac{eV}{kT}\right) - 1\right]$$

$$J_n = J_{TE}\left[\exp\left(\frac{eV}{kT}\right) - 1\right]$$ **Equation A4. 4**

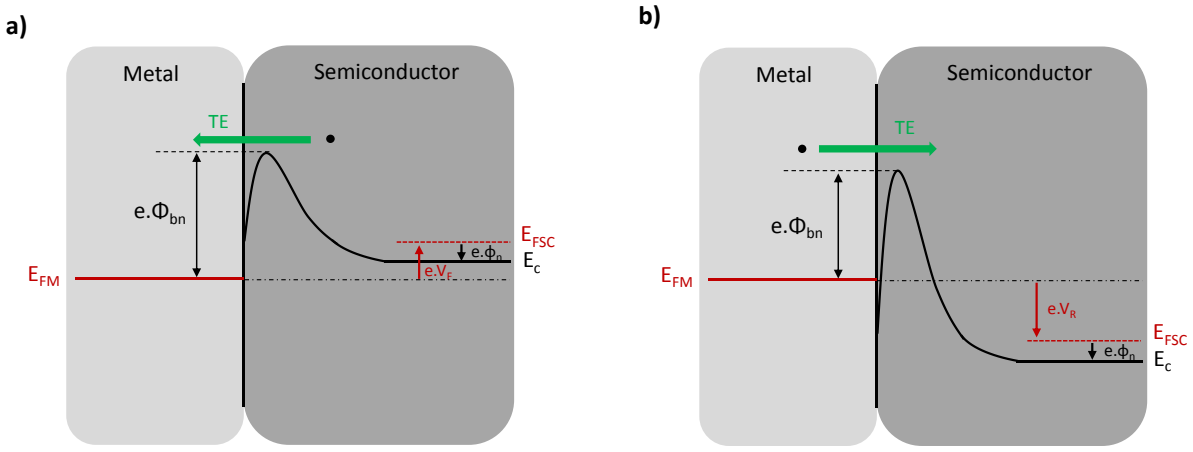


Figure A4. 2: Illustration of the TE conduction mode in a M/n-SC contact under (a) forward bias and (b) reverse bias.

The Drift / Diffusion theory

The diffusion theory was firstly proposed by Schottky in 1938 and is derived from the following assumptions [12]:

- The Schottky barrier height $e.\phi_{bn}$ must be larger than kT, where k is the Boltzmann constant and T the absolute temperature (kT = 26meV @ 300 K);
- The effect of electron collisions within the depletion region is included;
- The carrier concentration at x = 0 and x = W_{dep} are not affected by the current flow (they have their equilibrium value);
- The impurity concentration of the semiconductor is non degenerate.

Generally speaking, the current fluxes result from the displacement of charge carriers under a force. In the case of the drift / diffusion theory, the latter can be due to the presence of an electric field E(x) (drift) and/or from a concentration gradient (diffusion). According to this theory, the current density in the space charge region is given by:

$$J_n = e.\mu_n.n(x).E(x) + e.D_n\frac{\partial n}{\partial x}$$ **Equation A4. 5**

The use of this equation is valid under the assumption that the mobility of the charge carriers and the diffusion coefficient are independent from the electric field.

Using the Einstein relation ($\frac{D_n}{\mu_n} = \frac{kT}{e}$) and the expression that links the electric field to the polarization ($\vec{E} = -\vec{\nabla}V$), Equation A4. 5 can also be written as:

$$J_n = e.D_n\left[-\frac{e.n(x)}{kT}.\frac{\partial V(x)}{\partial x} + \frac{\partial n}{\partial x}\right]$$ **Equation A4. 6**

The integration of Equation A4. 6 over the space charge region (between 0 and W_{dep}) using $\left[\exp\left(-\frac{eV}{kT}\right) - 1\right]$ as an integrating factor leads to:

$$J_n = \left.e.N_C.D_n\left[\exp\left(\frac{eV}{kT}\right) - 1\right]\right/\int_0^{W_{dep}} exp\left[-\frac{eV(x)}{kT}\right].dx$$ **Equation A4. 7**

For a Schottky barrier, neglecting the image-force, the potential is:

$$V(x) = \frac{e.N_D}{\varepsilon_s}\left(W_{dep}.x - \frac{x^2}{2}\right) - \phi_{bn}$$ **Equation A4. 8**

With W_{dep} the width of the depletion layer:

$$W_{dep} = \sqrt{\frac{2.\varepsilon_s}{e.N_D}.\left(V_{bi} - V - \frac{kT}{e}\right)}$$ **Equation A4. 9**

Combining Equation A4. 7, Equation A4. 8 and Equation A4. 9 gives access to the drift/diffusion current expression:

$$J_n = \frac{e^2.D_n.N_C}{kT}.\left[\frac{e.(V_{bi} - V)2.N_D}{\varepsilon_s}\right]^{1/2}.exp\left(-\frac{e.\phi_{bn}}{kT}\right).\left[exp\left(\frac{e.V}{kT}\right) - 1\right]$$ **Equation A4. 10**

$$J = J_D.\left[exp\left(\frac{e.V}{kT}\right) - 1\right]$$

This current density expression is very similar to the thermionic one (Equation A4. 4). However, contrary to the saturation current density in the case of the thermionic theory, J_{TE}, J_D depends on the

applied voltage. The latter also varies less rapidly with the temperature than its thermionic counterpart.

The combined thermionic emission / diffusion theory

The main difference between the thermionic emission and the diffusion lies in the behavior of the quasi-Fermi level of electrons. In the diffusion theory, the charge carriers' concentration of the semiconductor immediately adjacent to the interface is assumed not to be modified by the polarization. This is similar to implying that the semiconductor quasi-Fermi level corresponds to that of the metal at the interface. In this case, it must decrease in the space charge region as represented by the dots in Figure A4. 1. On the contrary, the thermionic theory relies on the hypothesis that the Fermi level is constant in the space charge region all the way to the interface. In this case, the electrons situated in the semiconductor are not in equilibrium with those of the metal as their energy is higher. They are therefore considered as hot electrons. When the latter penetrate the metal, they get rid of their excess energy thanks to the collisions they undergo with the other conduction electrons and with lattice of the metal. Thanks to this process they reach equilibrium with the electrons of the metal and the two Fermi levels are aligned. This situation is schematically represented in Figure A4. 1 by the dashed line.

In sum, the gradient of the quasi-Fermi level providing the driving force for electrons to move, both theories rely on very different assumptions. In the case of the drift / diffusion theory, the main limitation for the current flow stands in the combined effects of drift and diffusion in the charge space region. On the contrary, according to the thermionic emission theory, the limiting process is the emission of electrons into the metal.

As a matter of fact the behavior of the charge carriers can be described by a combination of both theories: the thermionic emission / diffusion theory (TE-D). It was well described by Crowell and Sze, and taking into account the backscattering, quantum mechanical tunneling and reflection processes, the complete J-V characteristics is [13], [9]:

$$J(V) = A^{**}.T^2.\exp\left(-\frac{e.\phi_{bn}}{kT}\right).\left[exp\left(\frac{eV}{kT}\right)-1\right]$$

$$A^{**} = \left(\frac{f_p f_Q A^*}{1+\frac{f_p f_Q v_r}{v_d}}\right) \qquad \textbf{Equation A4. 11}$$

$$J(V) = J_{TED}.\left[exp\left(\frac{e.V}{kT}\right)-1\right]$$

The term $f_p = \exp(-x_m/\lambda)$ represents the probability of electron emission over the barrier where x_m is the position of the potential maximum from the interface and λ is the electron mean free path. The term f_Q represents the ratio of current flow taking into account the quantum mechanical tunneling and reflection to the current flow neglecting these effects.

Field-Effect emission (FE, TFE)

General description of the FE and TFE conduction modes

In the previous section we presented the conductions modes in which the charge carriers go from one side of the barrier to the other by getting over it. This kind of processes are well adapted for moderately doped semiconductors in forward bias were the TE mode is dominant. However, in many cases, and especially under reverse bias, a non-negligible part of the charge carriers tunnel through the barrier. This process allows the electrons that have an energy lower than that of the barrier to cross it. Two main situations can arise in that case under forward and reverse bias, and are schematically represented in Figure A4. 3.

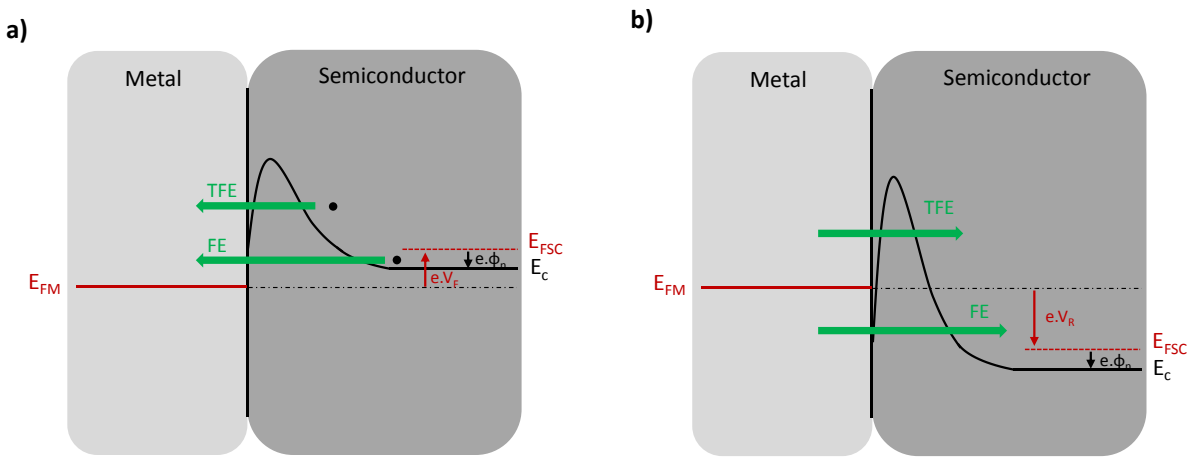


Figure A4. 3: Illustration of the FE and TFE conduction modes in a M/n-SC contact under (a) forward bias and (b) reverse bias.

In highly doped semiconductors, *i.e.* in degenerate semiconductors, and in forward polarization, the current mainly results from the tunneling of electrons with energies lower than the Fermi level of the semiconductor. This process corresponds to the field emission (FE) as described in Figure A4. 3. The ohmic characteristic of I(V) curves (linear dependence of I as a function of V) of contacts to heavily doped semiconductors often results from an important tunneling across a Schottky barrier. When increasing the temperature, some electrons are promoted in higher energy levels. Because of the quasi-triangular shape of the barrier, the probability of tunneling increases for these charge carriers as the barrier gets thinner. This phenomenon, called thermionic field emission (TFE) is schematically

represented in Figure A4. 3. If the temperature is further raised, some charge carriers might reach an energy high enough to go over the barrier (TE).

Discrimination of the dominant conduction mode

Models were established to discriminate the dominant transport mechanism considering that the electron flow can always be described by one of them [14], [15]. To do so, the quantity E_{00} was introduced:

$$E_{00} = \frac{e.\hbar}{2}\sqrt{\frac{N_d}{m_T^*.\varepsilon_s}} \qquad \textbf{Equation A4. 12}$$

- $E_{00} \ll kT$, the TE is considered as the dominant mechanism;
- $E_{00} \gg kT$, the FE is considered as the dominant mechanism;
- $E_{00} \approx kT$, TFE is considered as the dominant mechanism.

Forward bias (V_F)

Under forward bias, the FE current can be expressed as:

$$J_{FE} = \frac{A^{**}.T.\pi.\exp[-e(\phi_{bn} - V_F)/E_{00}]}{c_1.k.\sin(c_1\pi kT)}.[1 - \exp(-c_1.e.V_F] \qquad \textbf{Equation A4. 13}$$

With

$$c_1 \equiv \frac{1}{2E_{00}}.log\left[\frac{4(\phi_{bn} - V_F}{-\phi_n}\right] \qquad \textbf{Equation A4. 14}$$

Note that the quantity ϕ_n is negative in the case of a degenerate semiconductor such as represented in Figure A4. 3.

The TFE current can be expressed as:

$$J_{FE} = \frac{A^{**}T\sqrt{\pi.E_{00}e(\phi_{bn} - \phi_n + V_F)}}{k.\cosh(E_{00}/kT)}.exp\left[-\frac{e\phi_n}{kT} - \frac{e(\phi_{bn} - \phi_n)}{E_0}\right].\exp\left(\frac{e.V_F}{E_0}\right) \qquad \textbf{Equation A4. 15}$$

With

$$E_0 = E_{00}.\coth\left(\frac{E_{00}}{kT}\right) \qquad \textbf{Equation A4. 16}$$

Under reverse bias (V_R)

The FE current is given by:

$$J_{FE} = A^{**}\left(\frac{E_{00}}{k}\right)^2\left(\frac{\phi_{bn}+V_R}{\phi_{bn}}\right).exp\left(-\frac{2e\phi_{bn}^{3/2}}{3E_{00}\sqrt{\phi_{bn}+V_R}}\right)$$ **Equation A4. 17**

And the TFE current is given by:

$$J_{TFE} = \frac{A^{**}T}{k}\sqrt{\pi.E_{00}.e.\left[V_R+\frac{\phi_{bn}}{cosh^2\left(\frac{E_{00}}{kT}\right)}\right]}.\exp\left(-\frac{e.\phi_{bn}}{E_0}\right).\exp\left(\frac{e.V_R}{\varepsilon'}\right)$$ **Equation A4. 18**

With

$$\varepsilon' = \frac{E_{00}}{E_{00}/kT-\tanh(E_{00}/kT)}$$ **Equation A4. 19**

Discussion

The above mentioned equations give a very interesting qualitative insight but appear to be limited for a quantitative approach. Indeed, plotting the I(V) curves thanks to them reveals a computation problem in Padovani and Stratton's model. As pointed out by Crowell, the reverse bias expression does not go through zero at V=0 which results in the fact that the forward and the reverse bias do not connect [14].

Moreover, it was demonstrated that the comparison of E_{00} and kT presents strong limitations for the determination of the dominant transport mode [14]. Indeed, considering that the overall conduction is only due to one of the modes is an important approximation as it often results from a combination of all of them [16]. For example, L. Hutin showed that the proportion of tunneling current in a contact presenting a Schottky barrier height of 0.25 eV to p-Si doped at 2.10^{20} cm^{-3} (V_F = -1 V) is only of 61 % [16].

A5. Transmission Line Model (TLM) and specific contact resistivity extraction [Chapter 4]

TLM equations transposed to a contact

The Transmission Line Model presented in this appendix is that of Berger *et al* [17]. Based on transmission line equations the electrical behavior of contacts is described [18, 19, 20].

The original transmission line equations can be expressed in the frequency domain:

$$\frac{dV}{dx} = -(jwL + R).I \qquad \textbf{Equation A5. 1}$$

$$\frac{dI}{dx} = -(jwC + G).V \qquad \textbf{Equation A5. 2}$$

with L the distributed inductance, R the distributed resistance, C the capacitance and G the conductance.

A comparison between a transmission line and the contact, as represented in Figure A5. 1 leads to the following assumptions:

- The semiconductor layer corresponds to the series resistance R' of the transmission line;
- The interface resistance is the counterpart of the parallel shunt line conductance G';
- No inductance is considered, the latter being negligible compared with the series resistance even at high frequencies.

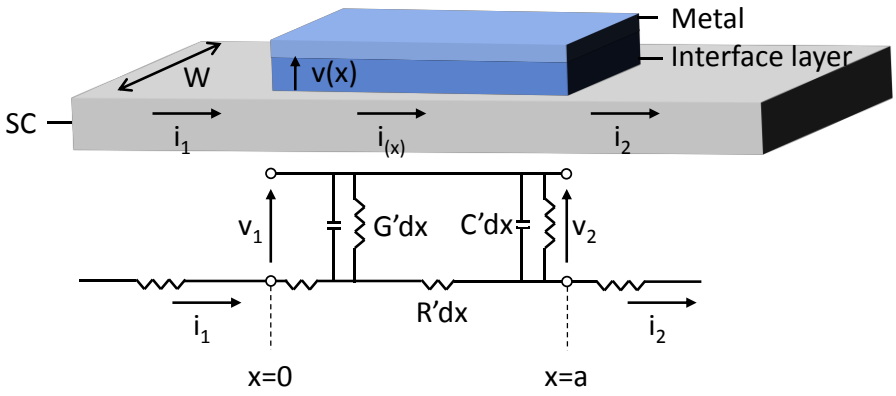


Figure A5. 1: Comparison of the contact region with a transmission line.

In this case, the line equations describe the current and voltage distribution along the contact:

$$\underline{V}(x) = \underline{V_1}\cosh(\gamma x) - \underline{I_1}.\underline{Z}\sinh(\gamma x) \quad \textbf{Equation A5. 3}$$

$$\underline{I}(x) = I_1\cosh(\gamma x) - \underline{V_1}/\underline{Z}\,.\,\sinh(\gamma x) \quad \textbf{Equation A5. 4}$$

With $\underline{Z}$ the characteristic impedance $\underline{Z} = \sqrt{\frac{R}{G}} = \frac{1}{w}\sqrt{R_{SK}.\rho_C}.\frac{1}{\sqrt{1+j.w.C^*.\rho_C}}$

And γ the propagation constant $\gamma = \alpha + j\beta = \sqrt{R.\underline{G}} = \sqrt{\frac{R_{SK}}{\rho_C}}\,.\sqrt{1+j.w.C^*.\rho_C}.$

where w is the pulsation, $w = 2\pi.f$,

C^* is the capacitance per unit area,

ρ_C is the specific contact resistivity,

R_{SK} is the sheet resistance of the semiconductor underneath the contact.

In the case of a DC-polarization ($w \to 0$), these equations can be written:

$$v(x) = v_1\cosh(\alpha x) - i_1.Z.\sinh(\alpha x) \quad \textbf{Equation A5. 5}$$

$$i(x) = i_1\cosh(\alpha x) - v_1/Z.\sinh(\alpha x) \quad \textbf{Equation A5. 6}$$

With

$$Z = \frac{1}{w}\,.\sqrt{R_{SK}.\rho_C} \quad \textbf{Equation A5. 7}$$

$$\alpha = \sqrt{\frac{R_{SK}}{\rho_c}} = \frac{1}{L_T} \quad \textbf{Equation A5. 8}$$

Where L_T is the transfer length.

Expression of the contact resistance

In the case of a TLM experiment, (see section 4.3. The Transfer Length Method) the total resistance between two probed contacts is:

$$R_{tot} = 2.R_C + R_{SH}.\frac{l_i}{W} \quad \textbf{Equation A5. 9}$$

Where R_C is the contact resistance and R_{SH} is the sheet resistance of the bulk semiconductor. Provided that the underlying semiconductor has been patterned in order to limit the crowding effect, the integrality of the injected current goes through the contact. Then, the contact resistance can be defined as:

$$R_c = \left.\frac{v_1}{i_1}\right|_{i_2=0}$$ **Equation A5. 10**

Therefore, combining Equation A5. 10, Equation A5. 5and Equation A5. 6:

$$R_c = Z.cth(\alpha a)$$ **Equation A5. 11**

Finally, replacing Z and α by their expressions:

$$R_c = \frac{\sqrt{R_{SK}.\rho_C}}{W}.cth(\frac{a}{L_T})$$ **Equation A5. 12**

$$R_c = \frac{R_{SK}.L_T}{W}.cth(\frac{a}{L_T})$$ **Equation A5. 13**

Expression of the specific contact resistivity

The extraction of the specific contact resistivity requires the use of a mathematical trick on Equation A5. 13. The latter leads to:

$$R_c = \frac{R_{SK}.L_T.L_T}{W.L_T}.cth(\frac{a}{L_T})$$ **Equation A5. 14**

Using the fact that $R_{SK}.{L_T}^2 = \rho_C$, Equation A5. 14 can be written:

$$R_c = \frac{\rho_C}{W.L_T}.cth(\frac{a}{L_T})$$ **Equation A5. 15**

As a consequence, one can express the specific contact resistivity:

$$\rho_C = \frac{R_C.L_T.W}{cth(a/L_T)}$$ **Equation A5. 16**

Expression of the end resistance

The end resistance R_E is defined as the drop of voltage $v_2 = v(a)$ divided by the input current i_1 for i_2 = 0.

$$R_E = \left.\frac{v_2}{i_1}\right|_{i_2=0}$$ **Equation A5. 17**

Combining Equation A5. 4, Equation A5. 5 and Equation A5. 17:

$$R_E = \frac{Z}{\sinh(\alpha a)}$$ **Equation A5. 18**

Finally, replacing Z and α by their expressions:

$$R_E = \frac{R_{SK}.L_T}{W}.\frac{1}{\sinh(a/L_T)}$$ **Equation A5. 19**

The relation linking R_E and R_C is finally:

$$\frac{R_C}{R_E} = cosh(\frac{a}{L_T})$$ **Equation A5. 20**

APPENDIX - Bibliographic references

[1] B. Castellon, “L’ellipsométrie spectroscopique,” *SOPRA - les fondamentaux*.

[2] N.-E. Ghellai, N. Benmansour, and A. Chabane Sari, “Ellipsométrie spectroscopique,” *Photoniques*, pp. 22–27, February 2011.

[3] M. N. Sestak, “Spectroscopic ellipsometry characterization of thin films used in the food packaging industry,” *American Laboratory*, 2013.

[4] H. J. Yvon, “TN11: Tauc-Lorentz dispertion formula,” *Horiba technical note*, 2006.

[5] H. Fujiwara, *Spectroscopic Ellipsometry: Principles and applicationS*. John Wiley & Sons, Ltd, 2007.

[6] V. Semiconductor, “The general properties of Si, Ge, SiGe, SiO2 and Si_3N_4,” June 2002.

[7] M. Yazdanmehr, S.-J. Asadabadi, A. Nourmohammadi, M. Ghasemzadeh, and M. Rezvanian, “Electronic structure and bandgap of γ-Al_2O_3 compound using mBJ exchange potential,” *Nanoscale Research Letters*, vol. 7, no. 1, pp. 1–10, 2012.

[8] V. Rose and R. Franchy, “The band gap of ultrathin amorphous and well-ordered Al_2O_3 films on CoAl(100) measured by scanning tunneling spectroscopy,” *Journal of Applied Physics*, vol. 105, no. 7, 2009.

[9] S. Sze, *Physics of Semiconductor Devices*, vol. 3rd edition. 2007.

[10] H. Bethe *MIT Radiation Lab Report*, vol. 43-12, 1942.

[11] S. Tiwari, *Compound semiconductor device physics*. Academic Press, 1992.

[12] W. Schottky, “Halbleitertheorie der sperrschicht,” *Naturwissenschaften*, vol. 26, no. 52, pp. 843–843, 1938.

[13] C. Crowell and S. Sze, “Current transport in metal-semiconductor barriers,” *Solid-State Electronics*, vol. 9, no. 11, pp. 1035 – 1048, 1966.

[14] C. Crowell and V. Rideout, “Normalized thermionic-field (T-F) emission in metal-semiconductor (schottky) barriers,” *Solid-State Electronics*, vol. 12, no. 2, pp. 89 – 105, 1969.

[15] F. Padovani and R. Stratton, “Field and thermionic-field emission in schottky barriers,” *Solid-State Electronics*, vol. 9, no. 7, pp. 695 – 707, 1966.

[16] L. Hutin, *Study of Schottky Barrier MOSFETs on SOI, SiGeOI and GeOI Substrates*. Theses, Institut polytechnique de Grenoble, Oct. 2010.

[17] H. Berger, “Contact resistance on diffused resistors,” in *Solid-State Circuits Conference. Digest of Technical Papers. 1969 IEEE Internationa*, vol. XII, pp. 160–161, 1969.

[18] H. Berger, “Models for contacts to planar devices,” *Solid-State Electronics*, vol. 15, no. 2, pp. 145 – 158, 1972.

[19] G. Reeves and H. Harrison, “Obtaining the specific contact resistance from transmission line model measurements,” *Electron Device Letters, IEEE*, vol. 3, no. 5, pp. 111–113, 1982.

[20] I. A. Smirnov and S. V. Kalinin, “Analysis of certain methods for determining contact resistivity,” pp. 162–164, 2011.

RESUME EN FRANÇAIS

INTEGRATION DE CONTACTS INNOVANTS POUR DISPOSITIFS PHOTONIQUES III-V/SI

Plan

Table des matières

Avertissement : Le résumé en français qui suit reprend les principales conclusions énoncées dans le manuscrit écrit en anglais et ne saurait donc être exhaustif.

CHAPITRE 1 INTRODUCTION A LA PHOTONIQUE SUR SILICIUM

1.1 Introduction générale

Depuis les années 2000, en raison d'une multitude de moyens de communication émergents, les besoins en termes d'échange de données n'ont cessé d'augmenter. Ces modifications ont conduit à l'initiation d'une transition depuis les technologies électroniques vers les technologies et interconnexions optiques. Entre autres, ces nouvelles technologies nécessitent l'utilisation de composants émetteurs et récepteurs de photons constitués de matériaux III-V. Ces derniers sont traditionnellement fabriqués et intégrés dans des salles blanches dédiées aux III-V pouvant traiter des plaques de 50 mm à 100 mm de diamètre avant d'être conditionnés dans des systèmes optoélectroniques. De façon à miniaturiser ces composants et à augmenter leurs performances tout en diminuant leur coût de fabrication, un modèle d'intégration innovant consiste à intégrer directement les sources III-V sur le circuit photonique silicium 200 mm. Jusqu'à maintenant, ce type de plaquette était alors détouré consécutivement au report du laser III-V de façon à recouvrer un diamètre de 100 mm maximum, et ainsi pouvoir être traité dans les salles blanches dédiées aux matériaux III-V. Dans le but de bénéficier de l'avantage économique que procure l'utilisation de l'expertise existant autour des technologies silicium, et ainsi de ne pas avoir à détourer les plaques, une intégration innovante est en cours de développement au sein de STMicroelectronics et du CEA-LETI dans le cadre de projets IRT Nanoelec. Ce tournant consiste à réaliser l'intégralité de l'intégration du laser III-V dans une salle blanche silicium 200 mm après son report sur le circuit photonique silicium. Afin d'optimiser les performances du laser III-V tout en respectant les contraintes liées à une salle blanche front-end / middle-end silicium, la réalisation d'une telle intégration nécessite notamment le développement de contacts innovants sur n-InP et p-InGaAs (Figure 1.1).

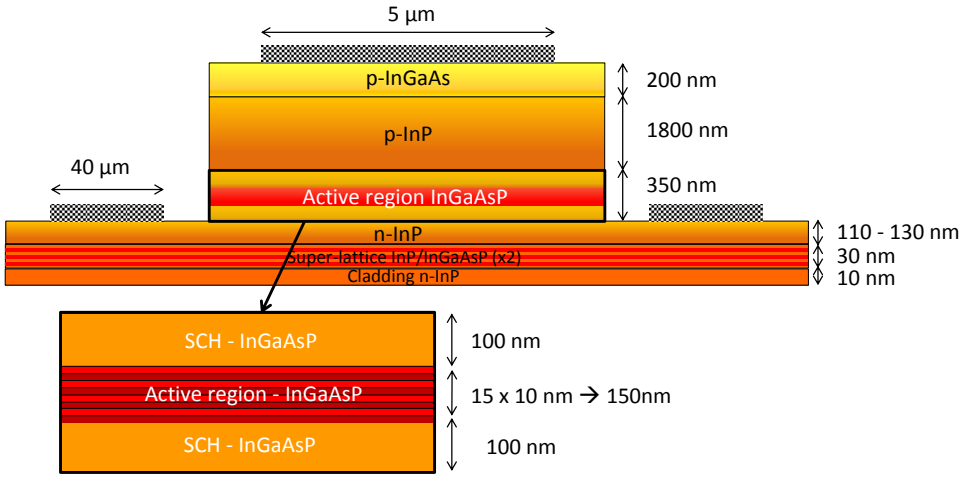


Figure 1.1 : Structure laser III-V utilisée par STMicroelectronics et le CEA-LETI. La dimension longitudinale du laser est de 500 µm.

Nous verrons par la suite que les contacts classiquement utilisés sur les lasers III-V jusqu'à présent ne sont pas compatibles avec un environnement silicium de par leur composition et leur intégration. De fait, une profonde refonte de ces contacts est nécessaire. Afin de pouvoir être intégrés au sein d'une plateforme silicium, tout en respectant les contraintes liées à un laser en fonctionnement, ces derniers doivent :

- Être intégrés sur des équipements compatibles silicium et pouvant traiter des plaques de 200 mm ou 300 mm de diamètre. Les procédés utilisés doivent permettre une intégration planaire des contacts, ce qui exclut tout procédé de type « lift-off » par exemple ;
- Le nombre d'étapes nécessaires à l'intégration des contacts doit être minimisée afin de minimiser de coût global de fabrication des composants ;
- Les contacts doivent être composés de matériaux compatibles avec un environnement silicium front-end / middle-end, comme par exemple Ni, Ti et leurs alliages ;
- L'ensemble des budgets thermiques doivent être minimisés ($T \leq 450$ °C) de façon à ne pas dégrader la région active du laser qui est composée de puits quantiques ;
- Les matériaux en contact avec / proches de la région active du laser ne doivent pas générer de pertes optiques trop importantes à la longueur d'émission du laser ($\lambda = 1{,}3 - 1{,}55$ µm) ;
- Les métallisations doivent être sélectionnées de façon à former des contacts présentant des résistivités spécifiques inférieures à $5.10^{-5}\ \Omega.cm^2$.

L'objectif de cette thèse est de développer des contacts innovants sur n-InP et p-InGaAs qui respectent l'ensemble de ces prérequis. Pour cela, il est tout d'abord nécessaire d'identifier sur quels principes de base repose le fonctionnement d'un laser III-V.

1.2 Le gain et les pertes optiques

La production de photons dans le laser III-V est basée sur l'émission stimulée de photons. Dans le cas du laser présenté en Figure 1.1, cette dernière est rendue possible grâce à la jonction P-N qui entoure la région active du laser, *i.e.* les puits quantiques. Par le biais d'un pompage électrique réalisé à l'aide des contacts qui sont repris de part et d'autre de la structure laser, l'émission de photons est réalisée. Cette dernière est initiée dès lors que le gain généré dépasse les pertes, c'est-à-dire dès lors que le gain seuil est atteint. Dans le cas de structures comprenant des puits quantiques composés de InGaAsP/InGaAs ou InGaAs/GaAs, le gain seuil est typiquement de 500 cm^{-1} alors que le gain maximum est de l'ordre de 3 x 10^3 cm^{-1} à 6 x 10^3 cm^{-1}.

Les pertes optiques quant à elles peuvent être dues à des phénomènes intrinsèques ou extrinsèques. On compte parmi elles :

- Les pertes par absorptions internes, qui correspondent à l'absorption de photons lors de transitions effectuées par les porteurs de charge ;
- Les pertes par dispersions, qui sont générées par les défauts rencontrés par les photons lorsqu'ils se propagent ;
- Les pertes générées par les matériaux métalliques et diélectriques se trouvant proches de la région active du laser ;
- Les pertes par radiations qui sont également générées par les matériaux diélectriques se trouvant proches de la région active du laser. Plus précisément, si les matériaux diélectriques présentent un indice de réfraction plus important que celui de la région active du laser, ils vont avoir tendance à extraire les photons de cette région et donc à générer des pertes.

1.3 Le pompage électrique du laser : les contacts repris sur n-InP et p-InGaAs

De façon à optimiser les performances du laser III-V, l'ensemble de ces pertes doit être minimisé alors que le gain doit lui, être maximisé à polarisation donnée. Les lasers étant utilisés par STMicroelectronics et le CEA-LETI étant pompés électriquement, l'un des développements cruciaux concerne les contacts qui sont intégrés de part et d'autre de la jonction P-N. De fait, comme l'électronique, la photonique requiert l'utilisation de contacts fiables et de qualité assurant des performances optimales à moyen et long terme. Dans ce cadre, les contacts sur III-V ont longuement été étudiés au cours des dernières décennies. Cependant, ces contacts que nous caractériserons de *classiques*, en opposition aux contacts *innovants* dont le développement fait l'objet de cette thèse, présentent de nombreuses limitations. La majorité d'entre eux requiert en effet des températures de recuit élevées (T ≥ 450 °C) ce qui aurait pour conséquence de dégrader la région active du laser et

donc de détériorer ses performances. De plus, outre les considérations purement liées au fonctionnement du laser, la co-intégration III-V / Si augmente considérablement le nombre de restrictions. En effet, alors que de nombreux contacts classiques sont constitués d'au moins une couche d'Au, ce composé est prohibé des salles blanches front-end / middle-end Si. Bien que des efforts aient été fournis afin de développer des contacts dépourvus d'Au, ils restent bien souvent composés de métaux nobles qui sont soit prohibés des salles Silicium front-end, soit trop couteux pour être implémentés dans l'industrie de masse. La majorité de ces contacts est également composée d'une multitude de matériaux (jusqu'à cinq pour certains) ce qui rend leur intégration complexe. Enfin, le schéma d'intégration de ces contacts classiques requiert l'utilisation de procédés non planaires tels que le lift-off à cause de la difficulté à polir et graver les métaux nobles. En conséquence, il apparait que les contacts classiques sont incompatibles avec un environnement front-end / middle-end Si de par leur composition et leur intégration. De fait, cette thèse est dédiée au développement de contacts innovants sur matériaux III-V. Le chapitre 2 présente ainsi le développement du schéma d'intégration de ces contacts sur n-InP et p-InGaAs au sein de salle blanche 200 mm du CEA-LETI dédiée aux technologies Si. La métallisation de contact, *i.e.*, la région ou le métal est en contact intime avec le semi-conducteur étant déterminante pour la réalisation de contacts ohmiques stables et reproductibles, les chapitres suivants lui sont dédiés. Le chapitre 3 traite ainsi tout d'abord de l'optimisation de cette métallisation de contact d'un point de vue métallurgique. Finalement, le chapitre 4 est dédié à l'étude électrique des contacts intégrés et plus précisément à l'impact de la nature de la métallisation en contact avec le III-V, ainsi qu'à l'impact de l'encapsulation diélectrique nécessaire à l'intégration planaire des contacts.

CHAPITRE 2 LE POMPAGE ELECTRIQUE DU LASER III-V : COMMENT INTEGRER LES CONTACTS DANS UN ENVIRONNEMENT COMPATIBLE SILICIUM ?

2.1 Intégration des contacts sur III-V au sein d'une salle blanche Si 200 mm

Comme nous l'avons expliqué précédemment, la co-intégration Si-III/V requiert le développement d'un schéma d'intégration pour les contacts au sein d'une salle blanche Si traitant des plaquettes de 200 mm de diamètre. Pour cela, nous avons mis en place différents outils de caractérisation qui sont plus précisément de nouveaux masques, dont le masque TASP (*TLM on Arsenide and Phosphorus-based surfaces*) qui permet l'intégration de contacts sur matériaux III-V exclusivement grâce à des équipements 200 mm. Ce masque embarque entre autres des structures de tests morphologiques qui ne sont autres que des réseaux de contacts de 5 µm x 5 µm tels que présentés en Figure 2.1.

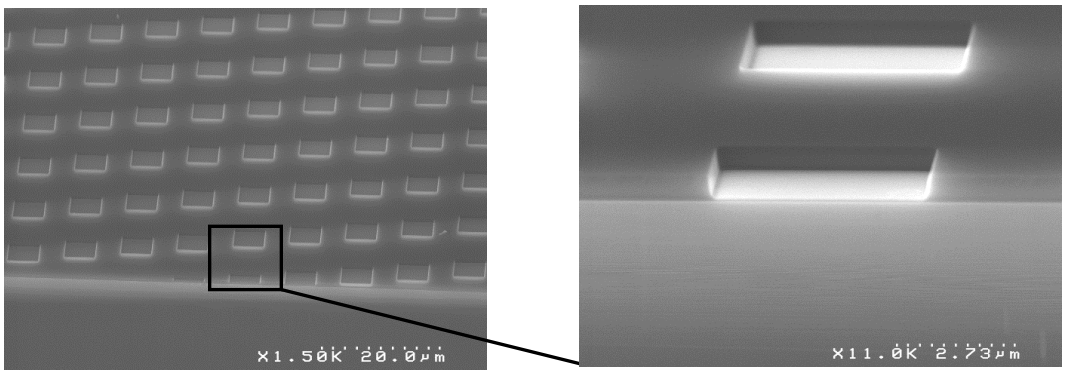


Figure 2.1 : Image MEB des structures morphologiques implémentées sur le masque 200 mm utilisé pour le développement du schéma d'intégration des contacts (TASP).

Les deux surfaces d'intérêt, *i.e.* n-InP et p-InGaAs se comportant de façon très différente les développements ont tout d'abord été conduits de façon indépendante. En revanche, dans un souci de cohérence, les empilements situés à l'aplomb de ces deux surfaces sont similaires à ceux présents dans le laser III-V et sont ainsi composés d'une alternance de couches d'InP, d'InGaAsP et d'InGaAs.

Le schéma d'intégration proposé et développé au cours du chapitre 2 est représenté schématiquement dans la Figure 2.2.

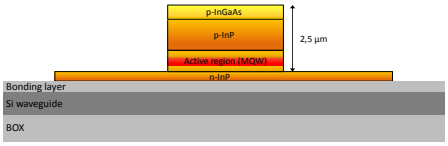
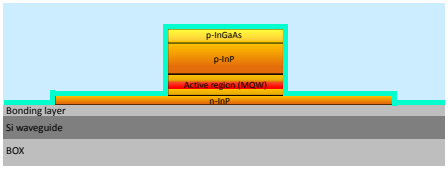
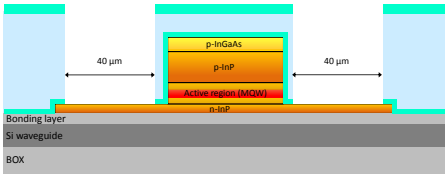
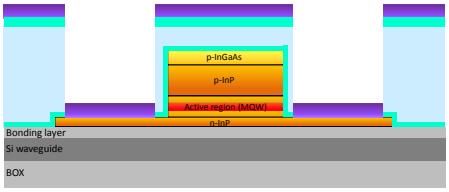
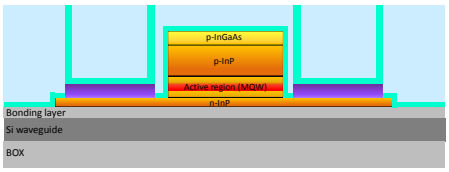
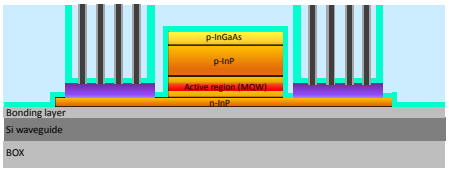
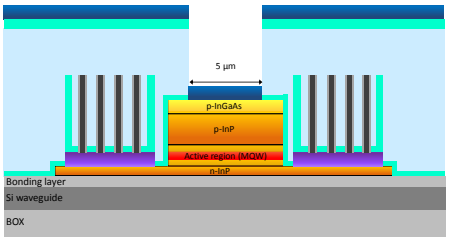
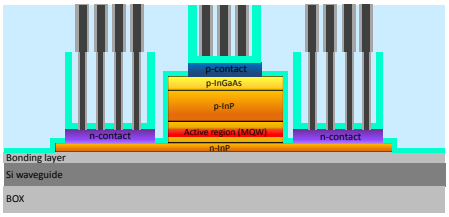
A		Gravure de l'empilement III-V et définition du laser
B		Encapsulation diélectrique Planarisation mécano-chimique (CMP)
C		Ouverture des cavités de contacts (1er niveau)
D		Préparation de surface (InP) Dépôt de la métallisation de contact
E		Dépôt de SiN et de matériau(x) diélectrique(s) Planarisation mécano-chimique (CMP) Traitement thermique (optionnel)
F		Ouverture des cavités de plugs (1er niveau) Préparation de surface et remplissage des plugs CMP damascène
G		Encapsulation diélectrique Ouverture des cavités de contacts (2nd niveau) Préparation de surface (InGaAs) Dépôt de la métallisation de contact
H		Dépôt de SiN et de matériau(x) diélectrique(s) Planarisation mécano-chimique (CMP) Traitement thermique (optionnel) Ouverture des cavités de plugs(2nd niveau) Préparation de surface et remplissage des plugs CMP damascène

Figure 2.2 : Représentation schématique de l'intégration de contacts sur un laser III-V dans le cadre de la photonique sur Silicium.

2.2 Détail des optimisations réalisées

L'ensemble de ces étapes a été optimisé afin de les adapter à des surfaces III-V qui réagissent très différemment du Si. L'ensemble des matériaux a également été choisi de façon à ne pas détériorer ces surfaces, mais aussi de façon à ne pas générer de pertes de photons qui pourraient altérer le rendement du laser.

2.2.1 Report de l'empilement III-V sur le substrat de Si

La première étape de l'intégration consiste à reporter l'empilement III-V sur le substrat Si 200 mm. Cette étape peut être réalisée à partir de plaques III-V de 50 mm ou 100 mm de diamètre. En revanche, à cause de l'importante perte de matière engendrée par cette solution, le report de puces millimétriques est à privilégier. Quelle que soit la voie choisie, ce report est réalisé par collage direct entre le III-V et une surface de Si oxydée au sein de STMicroelectronics et du CEA-LETI (Figure 2.3(a)). Le substrat d'InP qui servait à supporter l'épitaxie laser est alors retiré par voie chimique grâce à un mélange de HCl et de H_3PO_4 (Figure 2.3(b)).

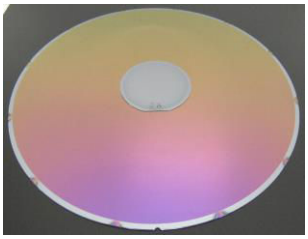
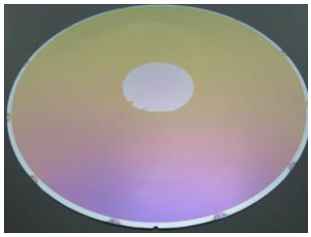
(a)  **(b)** 

Figure 2.3 : Photographie d'une plaque III-V (50 mm) reportée sur une plaque Si (200 mm) (a) après collage et (b) après retrait du substrat d'InP.

2.2.2 Gravure du laser III-V

Dès lors que l'empilement laser est reporté sur la plaque de Si 200 mm, le laser III-V doit être défini (cf Figure 2.2, étape A). Plusieurs micromètres de III-V devant être gravés pour révéler les surfaces d'InP sans dégrader l'InGaAs, cette étape nécessite l'utilisation d'un masque dur dont la composition et les conditions de dépôt doivent être choisies avec précaution. En effet, ce dernier est déposé sur les surfaces où les contacts vont par la suite être intégrés, et ne doit donc engendrer aucune détérioration du III-V. En ne déposant que quelques nanomètres des différents candidats disponibles, les études menées ont permis de démontrer que l'utilisation d'un masque dur composé de SiN conforme déposé par PE-CVD à 300 °C est tout à fait adaptée. Dès lors qu'il sera disponible dans la salle blanche front-end du CEA-LETI, un SiN low stress également déposé par PE-CVD à 300 °C permettra une amélioration additionnelle de cette étape d'intégration.

Comme nous l'avons déjà mentionné, la définition du laser en forme de T requiert la gravure de plusieurs micromètres de matière sur les flancs de l'empilement. De fait, l'utilisation de procédés de gravure anisotropes présentant de surcroit de hautes vitesses de gravure est nécessaire. Une gravure par voie chimique, qui présente un caractère isotrope serait donc tout à fait inadaptée. En revanche, il a été démontré qu'un plasma à couplage inductif (ICP) permet d'obtenir de hautes vitesses de gravure (260 à 360 nm/min) tout en générant des flancs verticaux et non rugueux. Ces attributs sont d'une importance primordiale dans le cadre du laser afin de ne pas générer des pertes par dispersion mentionnées dans le résumé du chapitre 1.

2.2.3 Encapsulation diélectrique

Dès lors que le laser est défini, une encapsulation diélectrique est requise afin de permettre une intégration planaire des contacts. Une première couche de diélectrique est tout d'abord déposée sur les surfaces III-V afin de constituer une couche d'arrêt à la gravure lors de l'ouverture des cavités de contact et ainsi de les protéger. Comme mentionné dans la section précédente, les études ont montré l'intérêt du SiN conforme déposé à 300 °C, ainsi que du SiN Low stress déposé à la même température. Dès lors, le choix du/des matériaux constituant le reste de l'encapsulation est primordial afin de ne pas générer de pertes optiques et afin de permettre une évacuation de la chaleur produite par le laser en fonctionnement. Le matériau sélectionné doit également être planarisable par CMP à cause de l'importante topographie que présente le laser III-V. Différents matériaux, *i.e.* SiN low stress, SiN conforme, SiO_2 et Al_2O_3, ont été caractérisés par le biais de la mesure de leur indice optique, de leur coefficient d'absorption à la longueur d'onde d'émission du laser (λ = 1,3 – 1,55 µm) et de leur conductivité thermique. La prise en compte de tous ces paramètres a conduit à la sélection du SiO_2 déposé par PE-CVD pour l'encapsulation diélectrique du laser.

2.2.4 Ouverture des cavités de contact

Afin d'ouvrir les cavités de contact dans cet empilement diélectrique jusqu'au III-V, une gravure anisotrope doit de nouveau être utilisée. Alors que la gravure du SiO_2 n'est pas problématique, celle du SiN se trouvant à la base de l'empilement, et donc à la surface des matériaux III-V est délicate. En effet, cette gravure débouchant sur les III-V sur lesquels la métallisation de contact sera intégrée par la suite, elle ne doit pas dégrader leur état de surface. Les deux gravures sèches classiquement utilisées pour graver du SiN se trouvant à la surface d'une plaquette de Si, *i.e.* le CH_2F_2 et le SF_6, ont été testées sur InP et InGaAs. Il s'avère que toutes deux ont tendance à dépléter les surfaces d'InP et d'InGaAs respectivement en P et As. Le SF_6 induit additionnellement une augmentation de la rugosité

de surface de l'InGaAs alors que le CH_2F_2 n'a aucun impact sur la rugosité des deux surfaces. La solution proposée est donc de graver la majorité du SiN grâce à un plasma de CH_2F_2 qui s'avère être le moins invasif, et de terminer cette ouverture par une gravure chimique à base de HF dilué (0,1 %). Il est important de noter que cette gravure chimique présente un caractère isotrope et qu'elle ne devra donc être utilisée que pour graver les derniers nanomètres de SiN et ainsi préserver les surfaces III-V sans augmenter les dimensions des contacts.

2.2.5 Préparation de surface III-V et intégration de la métallisation de contact

Suite à l'ouverture des cavités, la métallisation de contact peut être intégrée sur le III-V ainsi révélé. Afin de supprimer les éventuels contaminants, particules et oxydes qui pourraient se trouver sur les III-V, une préparation de surface est conduite. Cette dernière est composée de deux étapes : une première préparation est réalisée par voie chimique ; une seconde préparation est réalisée grâce à un plasma, directement dans l'équipement de dépôt afin d'éviter toute remise à l'air et donc toute recroissance d'oxyde. Les études menées ont permis de montrer que l'utilisation d'une solution de HCl concentrée (HCl : H_2O = 1 : 2) ou diluée (HCl : H_2O = 1 : 10) couplée à un plasma d'Ar ou d'He est tout à fait adaptée à la préparation de l'InGaAs. En revanche, les surfaces d'InP sont beaucoup plus sensibles et requièrent l'utilisation d'une solution de HCl diluée et d'un plasma d'He afin de ne pas être dégradées.

Dès lors, la métallisation de contact peut être intégrée. Deux stratégies peuvent être suivies pour cela :

- La métallisation de contact (métal ou composé intermétallique) peut être directement déposée sur le matériau III-V et stabilisée par le biais d'un traitement thermique ;
- Un métal peut être déposé sur le III-V et soumis à un traitement thermique dans le but de former des composés intermétalliques par réaction avec le matériau III-V.

Chaque phase ainsi déposée / formée possédant des propriétés métallurgiques et électriques différentes, ces solutions ouvrent la voie à une optimisation des performances électriques des contacts intégrés. Comme cela a déjà été mentionné, du fait de leur disponibilité dans les salles blanches front-end / middle-end, les métallisations à base de Ni et de Ti ont été étudiées au cours de ces travaux de recherche. Des études approfondies concernant ces métallisations de contacts seront présentées dans les résumés des chapitres 3 et 4, respectivement en ce qui concerne leurs aspects métallurgiques et électriques.

2.2.6 Encapsulation de la métallisation et intégration des plugs

Afin de contacter électriquement les métallisations se trouvant en fond de cavités, des plugs sont finalement intégrés. L'intégration planaire de ces plugs est réalisée grâce à une étape de CMP dite damascène. Ce procédé est hautement dépendant de la dimension des contacts et de leur densité : une densité trop importante générerait un phénomène d'érosion et des dimensions trop importantes (> 5 – 10 µm) donneraient lieu à un sur-polissage appelé dishing. Les contacts mesurant 40 µm x 500 µm sur n-InP et 5 µm x 500 µm sur p-InGaAs, l'intégration des plugs requiert de nouvelles cavités, plus petites. De fait, une nouvelle encapsulation diélectrique est réalisée en SiO_2 suite à quoi de nouvelles cavités sont ouvertes jusqu'à la métallisation de contact. Une fois ces cavités ouvertes, une couche de nucléation agissant également en tant que barrière à la diffusion du F est déposée. Cette dernière est classiquement composée de Ti/TiN déposée par CVD, mais une solution innovante consiste à déposer une fine couche de W dépourvu de F. Cette solution permet de diminuer la résistivité de la couche en question de 50 % à 60 % et ouvre ainsi la voie à une diminution de la résistance globale du contact intégré. Dès lors que ce liner est déposé sur les flancs et au fond des cavités, le métal de remplissage composé de W est déposé par CVD.

Un exemple de contact entièrement intégré grâce à ce schéma innovant est donné en Figure 2.4.

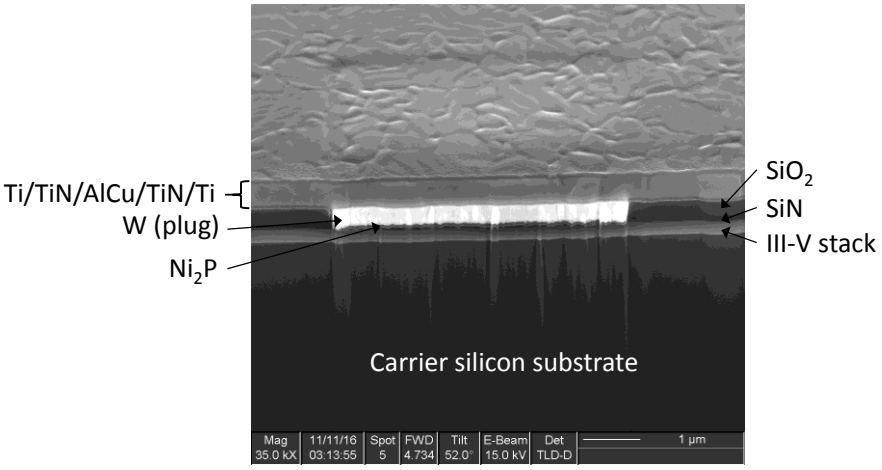


Figure 2.4: Image MEB d'un contact intégré sur n-InP avec une métallisation Ni_2P. La dimension de la cavité de contact présentée est de 5 x 5 µm et a donc permis une intégration directe du plug W sur la métallisation.

CHAPITRE 3 ÉTUDE METALLURGIQUE DES METALLISATIONS COMPATIBLES SILICIUM SUR N-INP ET P-INGAAS

Comme mentionné précédemment, la métallisation de contact est déterminante pour la formation de contacts ohmiques, stables en température et reproductibles. De fait, le chapitre 3 est dédié à l'étude métallurgique de cette région.

3.1 Procédure expérimentale

Au cours de ce chapitre, la formation de composés intermétalliques par réaction à l'état solide entre un métal et un semi-conducteur III-V est étudiée, avec plus précisément les systèmes suivants : Ni/n-InP, Ni/p-InGaAs et Ti/n-InP. Les substrats utilisés sont constitués d'une épitaxie de 300 nm d'InP (dopée Si : $N_D = 3 \times 10^{18}$ cm^{-3}) ou d'InGaAs (dopée Zn : $N_A = 3 \times 10^{19}$ cm^{-3}) située sur un substrat d'InP non dopé. Après avoir conduit une préparation de surface en deux temps (HCl concentré + pre-clean Ar^+), les couches de Ni ou de Ti (20 nm) sont déposées par PVD respectivement à température ambiante et à 100 °C. Les couches sont systématiquement capées par du TiN (7 nm) déposé par PVD à 100 °C afin d'empêcher toute contamination du film. Par la suite, les systèmes sont recuits soit par recuit rapide sous N_2 (RTP – 60 secondes) à des températures allant de 250 °C à 550 °C, soit par des recuits longs sous vide (plusieurs heures) composés de montées en températures jusqu'à 250 °C ou 340 °C (1,5 °C/min). Les systèmes ont par la suite été caractérisés en termes de morphologie et de composition de façon à identifier les séquences de phases ainsi que les mécanismes associés à l'apparition des différents composés intermétalliques.

3.2 Étude métallurgique du système Ni/InP

L'étude menée sur le système Ni(20 nm)/n-InP a permis de montrer que la préparation de surface comprenant une solution concentrée de HCl (HCl : H_2O = 1 : 2) et un pre-clean Ar^+ in situ modifie l'état de surface de l'InP. Une couche amorphe présentant un gradient de concentration est ainsi créée à la surface de l'InP. Cette dernière est riche-In sur quelques nanomètres, riche P sur les nanomètres suivants avant de recouvrer sa stœchiométrie initiale. Après des recuits rapides et dès 300 °C, la séquence de phase identifiée met en jeu la coexistence de phases binaires et ternaires (Ni_2P, Ni_3P et Ni_2InP) dont la formation est associée à un rejet d'indium afin de conserver la stœchiométrie globale du système. L'augmentation de la température a pour effet de promouvoir la phase Ni_2P au dépend des phases Ni_3P et Ni_2InP. Ce phénomène est accompagné par l'apparition de la phase In cristalline dès 350 °C. Finalement, à 550 °C la morphologie des couches est extrêmement dégradée, le Ni_2P étant complétement aggloméré et entouré par la phase In à cette température. Les

différentes caractérisations mettent en exergue le fait que la formation des composés binaires et ternaires n'est pas contrôlée par la nucléation mais par la diffusion des différents composés et/ou par les réactions interfaciales. Au contraire, la formation de la phase In requiert une température minimale de 350 °C et est ainsi contrôlée soit par la nucléation soit par un phénomène de fusion / solidification, la température de fusion de l'In ayant largement été dépassée (T_F = 156 °C).

L'ensemble des résultats concernant le système Ni/InP est résumé schématiquement dans la figure Figure 3.1.

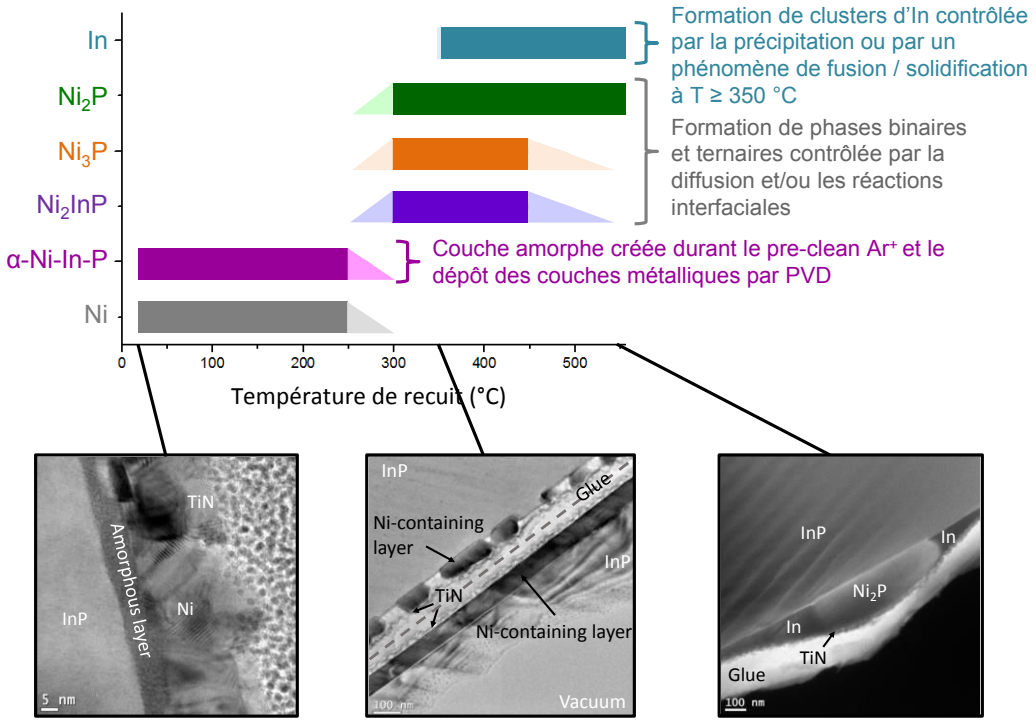


Figure 3.1 : Résumé graphique des principaux résultats obtenus sur le système Ni/InP.

3.3 Étude métallurgique du système Ni/InGaAs

Une étude similaire menée sur le système Ni/InGaAs a également permis d'identifier la séquence de phases, qui s'avère différente de la plupart des résultats reportés dans la littérature.

Tout d'abord, il apparait que contrairement aux surfaces d'InP, l'InGaAs n'est pas altéré par la préparation de surface conduite (HCl : Ar^+) et conserve ainsi son état initial. Le dépôt des couches de Ni et de TiN respectivement à température ambiante et 100 °C n'engendre pas la formation de composé cristallin. En revanche, deux régions où les espèces ont inter-diffusé ont été identifiées :

- Le Ni et le TiN coexistent sur une fiche couche d'environ 3 nanomètres ;
- Le Ni et l'InGaAs coexistent dans une région d'environ 25 nanomètres.

Il est important de noter que la stœchiométrie initiale de l'InGaAs est conservée dans cette seconde couche, ce qui suggère le fait qu'une réaction est initiée lors du dépôt grâce à la diffusion du Ni dans l'InGaAs. Par la suite, ce système est stable jusqu'à une température de 250 °C où aucun nouveau composé cristallin n'est identifié. En revanche, dès 350 °C, le Ni est entièrement consommé et une phase unique et uniforme est ainsi formée. Contrairement à la littérature qui reporte la formation du composé $Ni_2(In_{0.53}Ga_{0.47})As$, aussi noté $Ni_4InGaAs_2$, nous observons la formation de la phase hexagonale $Ni_3(In_{0.53}Ga_{0.47})As$. Comme cela avait déjà été observé après dépôt, la conservation de la stœchiométrie initiale de l'$In_{0.53}Ga_{0.47}As$ dans ce composé met en avant le fait que le Ni est l'espèce diffusante lors de la formation de cette phase. Une nouvelle augmentation de la température tend à dépléter cette phase en In et Ga, ce qui a pour effet de créer une phase NiAs-like à 550 °C qui est de surcroit complètement agglomérée à cette température. En revanche, malgré ce changement drastique de composition, le composé possède toujours une structure hexagonale.

L'ensemble des résultats concernant le système Ni/InGaAs est résumé schématiquement dans la figure Figure 3.2.

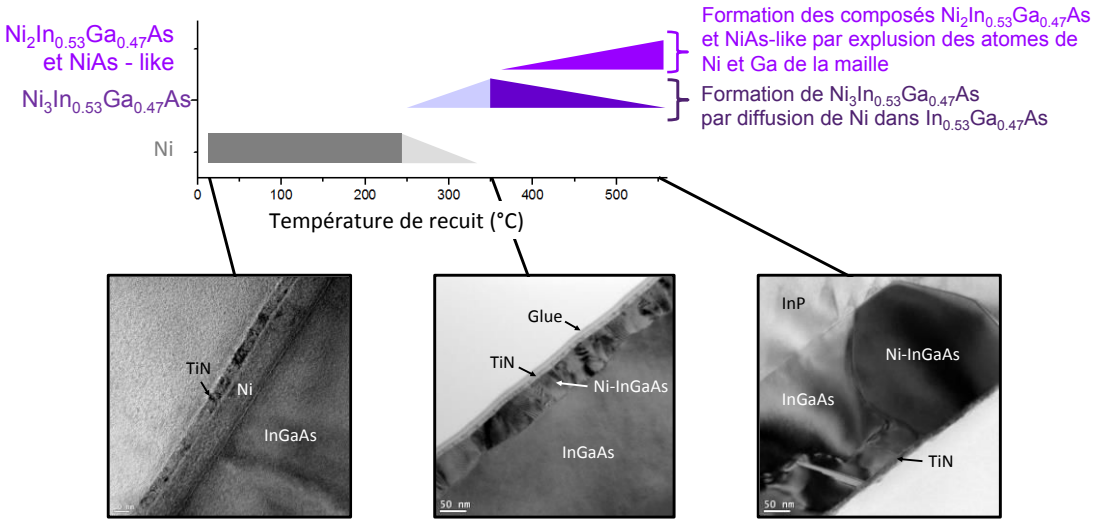


Figure 3.2 : Résumé graphique des principaux résultats obtenus sur le système Ni/InGaAs.

3.4 Etude métallurgique du système Ti/InP

Finalement, l'étude conduite sur le système Ti/InP a permis de mettre en exergue l'initiation d'une réaction entre le Ti et l'InP dès le dépôt des couches métalliques conduit à 100 °C. La formation simultanée de deux composés binaires, le TiP et le Ti_2In_5, est ainsi observée. Alors que le premier composé est largement reporté dans la littérature, le second n'avait encore jamais été observé. Nous attribuons cette différence au gradient de composition créé dans l'InP par la préparation de surface conduite en deux temps, avec tout d'abord une solution de HCl concentrée puis avec un pre-clean in

situ d'Ar^+. Grâce à leur énergie cinétique éventuellement combinée à un phénomène de diffusion, les atomes de Ti atteignent les zones riche-In et riche-P présentes à la surface de l'InP. De fait, une structure composée de couches distinctes est observée : TiN / Ti / Ti_2In_5 (7 à 15 nm) / TiP (3 à 8 nm) / InP. Il est important de noter que les épaisseurs des couches de Ti_2In_5 et de TiP ne sont pas parfaitement constantes au sein même d'un système, mais qu'elles sont entièrement indépendantes de l'épaisseur de Ti déposée. Dès lors que le TiP et le Ti_2In_5 forment des couches continues, au moins l'une d'entre elles agit en tant que barrière de diffusion empêchant de fait toute réaction jusqu'à 450 °C, bien qu'un important réservoir de Ti soit disponible. En accord avec la littérature, il est très probable que le TiP joue le rôle le plus important dans cette absence de réaction. Dans cette configuration, le Ti, le Ti_2In_5 et le TiP coexistent donc jusqu'à une température de 450 °C sous la forme de couches continues et distinctes. En revanche, un recuit conduit à 550 °C engendre la consommation complète du Ti et du Ti_2In_5 pour promouvoir le TiP ainsi que la phase In nécessaire à la conservation de la stœchiométrie du système. Cette réaction est rendue possible par la création d'un chemin de diffusion permettant au Ti et au P de se rencontrer, soit par la promotion de la diffusion des espèces à travers la couche de TiP ou par l'agglomération de cette couche.

L'ensemble des résultats concernant le système Ti/InP est résumé schématiquement dans la figure Figure 3.3.

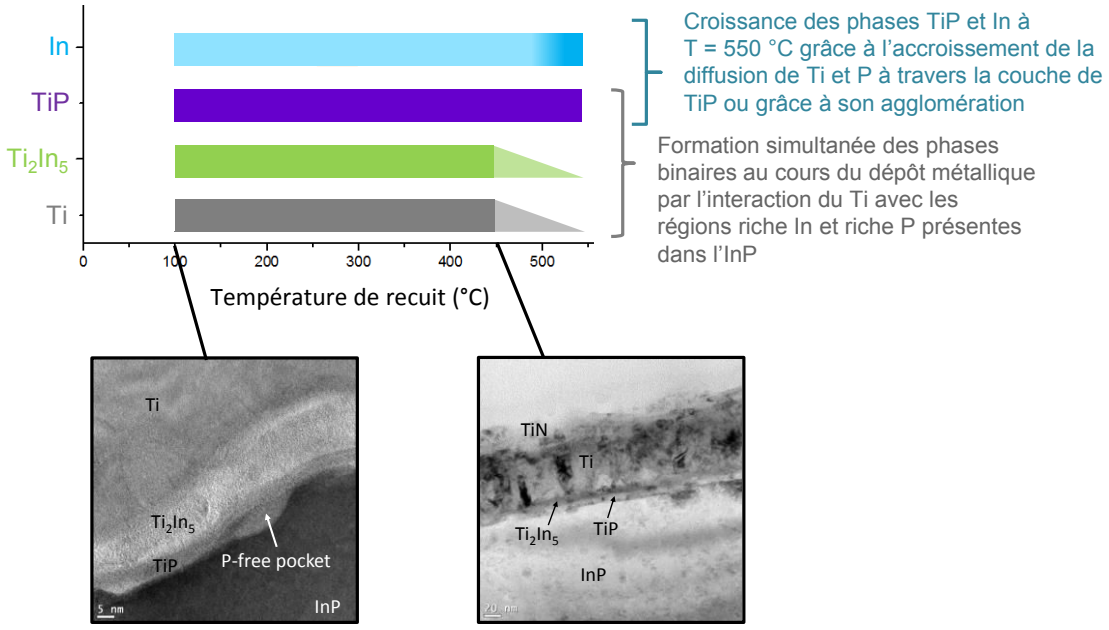


Figure 3.3 : Résumé graphique des principaux résultats obtenus sur le système Ti/InP.

CHAPITRE 4 CONTACTS COMPATIBLES SILICIUM SUR N-INP ET P-INGAAS : CARACTERISATION ELECTRIQUE

Le chapitre 4 est finalement dédié à l'étude électrique des contacts intégrés grâce à l'utilisation de structures de type TLM. Dans le cadre de la photonique sur Silicium, les contacts intégrés sur le laser III-V doivent être de type ohmiques entre -1.5 V et + 1.5 V et doivent présenter une résistivité spécifique de contact $\rho_C \leq 5 \times 10^{-5}\ \Omega.cm^2$.

4.1 Extraction de la résistivité spécifique de contact - Structures TLM

Afin d'extraire les résistivités spécifiques des contacts intégrés, des structures de type TLM (Transfer Length Method) sont utilisées. Elles sont constituées d'une série de contacts dont les dimensions sont constantes mais dont l'espacement augmente, comme représenté sur Figure 4.1.

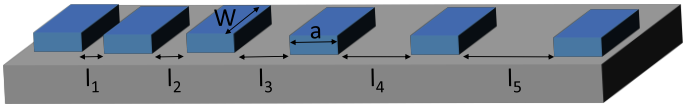


Figure 4.1 : Représentation schématique d'une structure de test TLM.

Chaque couple de contact adjacent est caractérisé grâce à une mesure 4 pointes permettant d'extraire la caractéristique I(V) correspondante. Par la suite, si les caractéristiques sont linéaires, *i.e.* si les contacts sont ohmiques, la résistance correspondant à chaque espacement est extraite et tracée en fonction des espacements correspondants comme représenté dans la Figure 4.2.

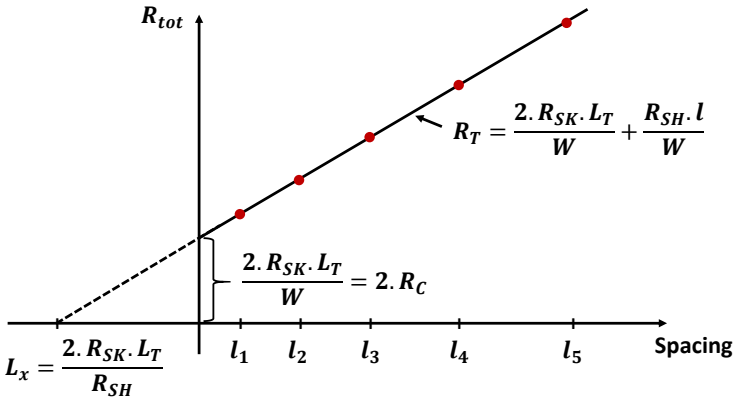


Figure 4.2 : Représentation schématique du tracé R(l) utilisé pour extraire la résistivité spécifique de contact dans le cadre d'une mesure TLM.

Dans le cas de contacts non-alliés, la résistivité du semi-conducteur bulk (R_{SH}) et celle du semi-conducteur situé sous le contact (R_{SK}) sont considérées comme étant égales. Dans ce cas, l'extraction de la résistivité spécifique de contact est immédiate à partir de ce tracé. En revanche, dans le cas de contacts alliés, une correction peut être appliquée afin de prendre en compte une éventuellement modification de la résistivité du semi-conducteur situé à l'aplomb du contact. Dans ce cas, des mesures supplémentaires sont nécessaires afin d'extraire un paramètre appelé résistance de fin (R_E). Dans ce chapitre, les limitations associées aux techniques d'extraction décrites dans la littérature sont largement discutées. Les deux méthodes disponibles reposent sur des hypothèses décrivant le chemin emprunté par les porteurs de charge, ainsi que sur la localisation des isopotentielles qui s'avèrent non vérifiées. De fait, ce type d'extractions engendre des erreurs conséquentes lorsqu'elles sont utilisées au sein de réseaux de contacts sans plus de corrections. Par conséquent, il a été décidé d'appliquer la méthode dédiée aux contacts non alliés pour extraire l'ensemble des résistivités spécifiques de contact présentées dans ce chapitre, cette dernière étant beaucoup plus fiable.

4.2 Étude des métallisations compatibles avec un environnement front-end middle-end Si

Tout d'abord, les métallisations à base de Ni et de Ti étudiées dans le chapitre 3 ont été caractérisées électriquement. Une métallisation supplémentaire, le Ni_2P a été directement déposé sur chacun des substrats d'intérêt. Les résistivités spécifiques de contact obtenues sur n-InP et p-InGaAs sont présentées respectivement dans la Figure 4.3 et dans la Figure 4.4.

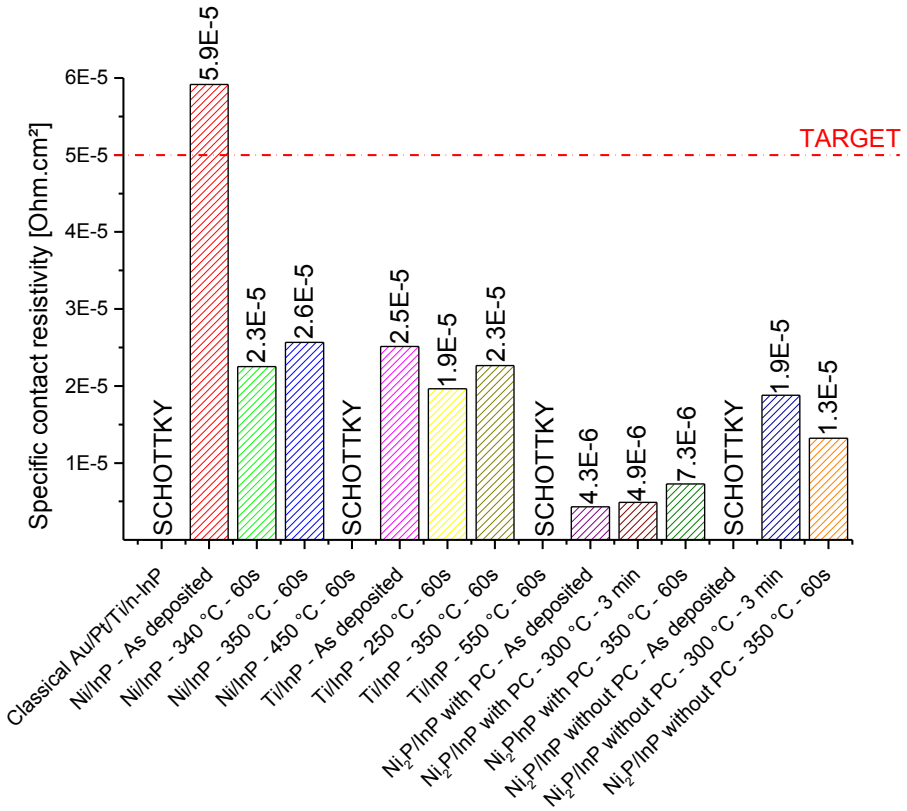


Figure 4.3: Résistivités spécifiques de contact obtenues avec des métallisations à base de Ni et Ti sur n-InP (N_D = 3 x 10^{18} cm^{-3}). Quand rencontré, PC signifie pre-clean Ar^+ in situ.

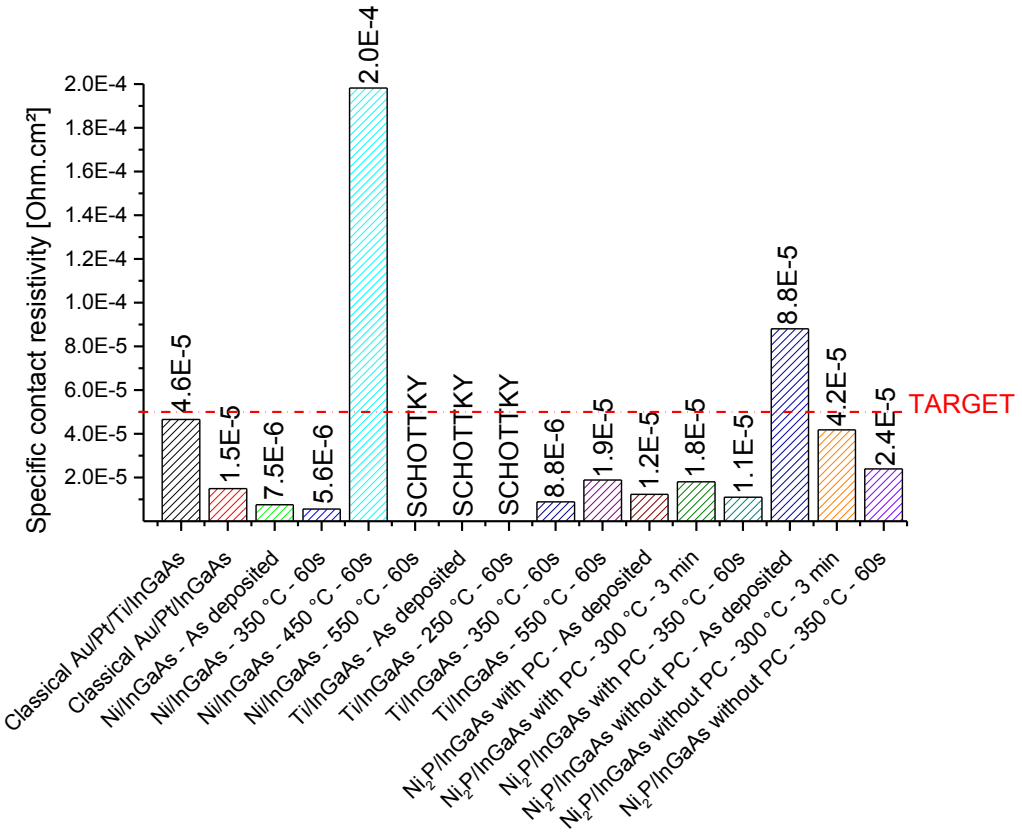


Figure 4.4: Résistivités spécifiques de contact obtenues avec des métallisations à base de Ni et Ti sur p-InGaAs (N_A = 3 x 10^{19} cm^{-3}). Quand rencontré, PC signifie pre-clean Ar^+ in situ.

Les résultats présentés ci-dessus mettent en avant le fait que la grande majorité des métallisations étudiées présentent de meilleures caractéristiques que les métallisations classiques sondées, et qu'elles pourraient tout à fait être implémentées sur des lasers III-V. Cependant, cette étude électrique combinée avec l'étude métallurgique présentée dans le chapitre 3 nous donne accès à une vue d'ensemble permettant de restreindre les choix aux plus pertinents. Pour cela, il est important de noter que l'intégration des contacts sur n-InP et p-InGaAs dans le laser peut être (i) séquentielle ou (ii) simultanée.

Dans le cas d'une ouverture simultanée des deux niveaux de contacts, le nombre d'étapes d'intégration serait drastiquement réduit. Si cette solution est finalement retenue, une métallisation unique doit être intégrée sur les deux semi-conducteurs d'intérêt. Afin d'obtenir le meilleur compromis, il convient réaliser un pre-clean in situ d'Ar^+, ou d'He lorsque ce dernier est disponible, et de déposer du Ni_2P. Cette solution permet ainsi d'atteindre des résistivités de contact de 4.3 x 10^{-6} $\Omega.cm^2$ and 1.2 x 10^{-5} $\Omega.cm^2$ respectivement sur n-InP et p-InGaAs. Ce type de métallisation présente également l'avantage d'être stable thermiquement au moins jusqu'à 350 °C sur chacun des semi-conducteurs, ce qui permet de fait à la métallisation de supporter les budgets thermiques appliqués au cours des étapes d'intégration suivantes.

Cependant, l'importante topographie présente entre les surfaces d'InP et d'InGaAs dans le laser rend cette intégration simultanée difficile. De fait, une intégration séquentielle des contacts est à envisager. Dans ce cas, chacune des deux métallisations peut être indépendamment optimisée, en faisant néanmoins extrêmement attention aux budgets thermiques requis afin de ne pas dégrader la première métallisation lors de l'intégration de la seconde. Dans ce cas, alors que le Ni_2P combiné à un pre-clean in situ d'Ar^+, ou d'He dans sa version optimisée, est le plus adapté à une surface de n-InP, l'utilisation du Ni minimiserait la résistivité de contact sur p-InGaAs. Chacune des métallisations peut être utilisée sans recuit, auquel cas l'ordre dans lequel elles sont intégrées n'aurait pas d'importance. En revanche, afin de minimiser autant que possible les résistivités de contacts sur chacun des semi-conducteurs, l'utilisation du Ni_2P tel que déposé sur n-InP et du Ni recuit à 350 °C pendant 60 secondes sur p-InGaAs constituerait la meilleure solution. Dans ce cas, il convient d'intégrer tout d'abord les contacts sur p-InGaAs et ensuite ceux sur n-InP. Cette solution permettrait d'atteindre les valeurs de ρ_C = 4.3 x 10^{-6} $\Omega.cm^2$ et ρ_C = 5.6 x 10^{-6} $\Omega.cm^2$ respectivement sur n-InP et p-InGaAs.

4.3 Impact de l'encapsulation diélectrique

Finalement, après avoir déterminé les métallisations les plus adaptées sur chacun des semi-conducteurs d'intérêt, l'impact du diélectrique nécessaire à l'intégration planaire des contacts a été caractérisé. Pour cela, des empilements classiques ont été utilisés et les diélectriques mentionnés

dans le chapitre 2 ont été déposés. De plus, l'intégration présentée dans le chapitre 2 nécessitant l'utilisation d'une couche d'arrêt à la gravure protégeant les III-V et étant composée de SiN, une telle couche a toujours été déposée dans les empilements étudiés dans cette section. Les cavités de contact ont alors été ouvertes jusqu'aux matériaux III-V grâce à une gravure sèche à base de SF_6. Les métaux constituants les empilements classiques ont alors été déposés par PVD à des températures n'excédant pas 100 °C. Trois échantillons supplémentaires constituants les références ont été intégrés de façon classique, c'est-à-dire sans diélectrique et grâce à des procédés de type lift-off. L'ensemble des résistivités spécifiques de contacts obtenues est présenté dans la Figure 4.5.

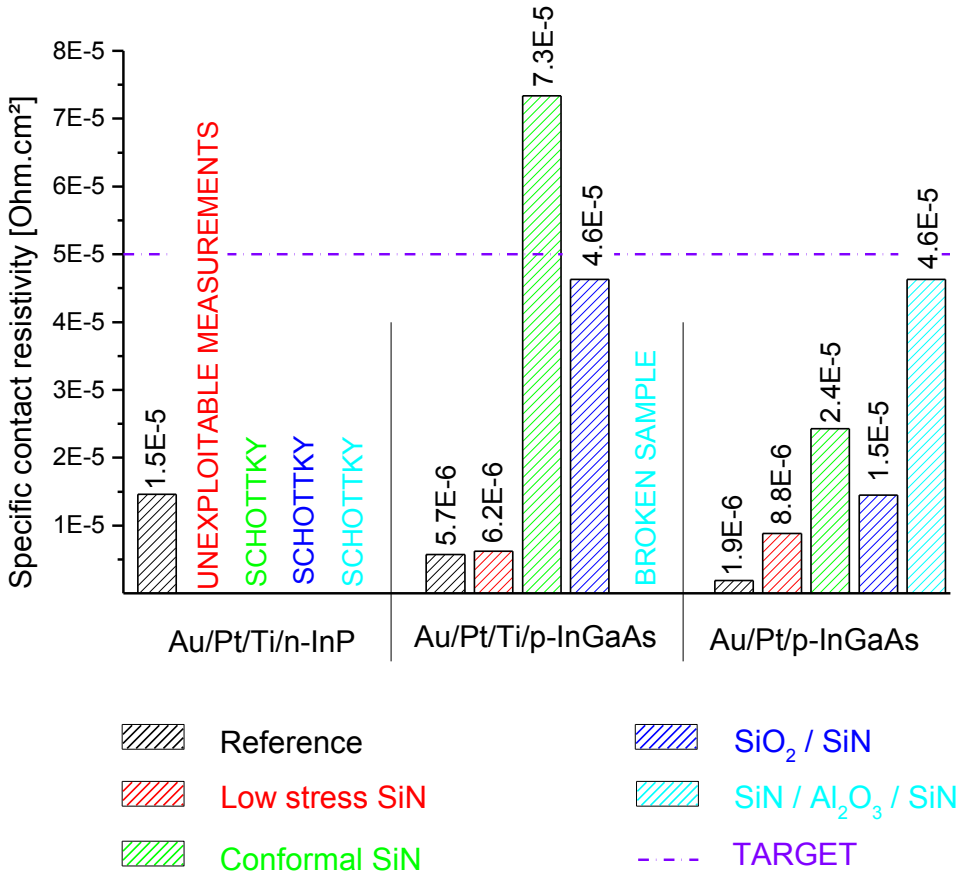


Figure 4.5: Résistivités spécifiques de contact obtenues avec des empilements classiques sur n-InP et p-InGaAs en fonction des encapsulations diélectriques utilisées.

Il s'avère que l'intégration planaire nécessitant le dépôt et la gravure d'un empilement diélectrique dégrade sans exception les performances électriques des contacts par rapport à celles obtenues avec une intégration basée sur le lift-off. Ces détériorations peuvent être attribuées en première instance à l'incorporation d'H dans les semi-conducteurs au cours du dépôt par PE-CVD du SiN utilisé en tant que couche d'arrêt à la gravure. En effet, la présence d'H dans les épitaxies dopées a pour effet de diminuer la concentration d'espèces dopantes actives. De plus, l'utilisation d'une gravure sèche basée sur un plasma de SF_6 a tendance à modifier l'état de surface de l'InP et de l'InGaAs en altérant leur stœchiométrie et leur rugosité. En revanche, ces hypothèses ne suffisent pas à expliquer les

différences observées lorsque la nature du diélectrique situé au-dessus de cette couche de SiN est modifiée. Ces variations peuvent cependant être attribuées au stress intrinsèque de ces composés diélectriques qui semblent avoir un impact direct sur les résistivités de contact extraites. Différents phénomènes peuvent en effet modifier la répartition des porteurs de charges situés proches d'ouvertures réalisées dans des empilements diélectriques contraints :

- Les dopants peuvent être redistribués dans le semi-conducteur à cause de la modification de la concentration des sites interstitiels et des lacunes dans la maille cristalline sous l'effet d'une contrainte ;
- Les diagrammes de bandes peuvent être déformés sous l'effet d'une contrainte ce qui a pour effet de modifier les mécanismes responsables du transport des porteurs de charges au sein de la jonction métal / semi-conducteur ;
- La présence d'une contrainte peut donner lieu à un effet piézoélectrique dans les matériaux III-V et ainsi générer une densité de charges additionnelle dans la région du contact.

CONCLUSION GÉNÉRALE

Au cours de cette thèse, les problématiques liées à l'intégration de contacts sur III-V dans un environnement front-end / middle-end Si 200 mm ont été discutées et des solutions ont été proposées. Pour cela, un schéma d'intégration de contacts sur n-InP et p-InGaAs a été développé au sein d'une telle salle blanche. Ce schéma requiert tout d'abord le report d'un empilement III-V sous forme de plaquette ou de puces par le biais d'un collage direct InP / SiO_2. Par la suite, le laser est défini dans cet empilement grâce à une gravure sèche réalisée avec un plasma à couplage inductif (ICP). Afin de protéger l'InGaAs, cette étape nécessite le dépôt d'un masque dur composé de SiN conforme déposé par PE-CVD à 300 °C, ou de SiN Low stress déposé de la même façon dans sa version optimisée. Les caractérisations métallurgiques et électriques ont montré que ce dernier permet de préserver les surfaces III-V tout en optimisant les performances électriques des contacts intégrés de façon planaire. Ce type d'intégration requiert alors une encapsulation diélectrique du laser afin de réaliser par la suite une CMP de type damascène. La nature de cette encapsulation diélectrique doit être choisie avec précaution afin de ne pas générer de pertes optiques à la longueur d'onde d'émission du laser (λ = 1,3 – 1,55 µm), afin de permettre une évacuation de la chaleur produite par le laser en fonctionnement et afin d'être planarisable par CMP. En prenant en compte l'ensemble de ces restrictions, le SiN low stress couplé avec du SiO_2 tous deux déposés par PE-CVD ont été sélectionnés. L'ouverture des cavités de contact dans cette encapsulation diélectrique est alors réalisée par le biais d'une gravure sèche. Alors que la gravure du SiO_2 n'est pas problématique, celle du SiN doit être réalisée avec beaucoup de précautions afin de ne pas dégrader les surfaces III-V sur lesquelles les contacts sont intégrés par la suite. Cette gravure sèche est alors réalisée grâce à un plasma de CH_2F_2 couplé à une solution de HF (0,1 %), cette dernière étant utilisée pour graver les derniers nanomètres de SiN. La préparation de surface alors conduite afin de supprimer toute trace de contaminants, particules et oxydes est composée d'une succession de deux étapes. Sur InGaAs, l'utilisation d'une solution de HCl concentrée ou diluée combinée avec un plasma d'Ar ou d'He est tout à fait adaptée, alors que la préparation de l'InP requiert l'utilisation d'une solution de HCl diluée combinée avec un plasma d'He. Dès lors, la métallisation de contact peut être intégrée (i) simultanément sur n-InP et p-InGaAs ou (ii) séquentiellement. (i) Dans le cas d'une intégration simultanée, l'utilisation de la métallisation Ni_2P précédée d'un pre-clean in situ optimisé permet d'obtenir le meilleur compromis sur chacun des deux semi-conducteurs. Les résistivités de contact ainsi atteintes sont de 4.3 x 10^{-6} Ω.cm^2 and 1.2 x 10^{-5} Ω.cm^2 respectivement sur n-InP and p-InGaAs. Cette métallisation présente également l'avantage d'être stable thermiquement au moins jusqu'à 350 °C. (ii) Dans le cas d'une intégration séquentielle des deux types de contacts, chacun peut être indépendamment optimisé. Le contact sur p-InGaAs doit alors être intégré le premier avec une métallisation Ni ayant subi un traitement thermique à 350 °C pendant 60 secondes. Ce type de

traitement thermique mène à la formation d'un phase unique et uniforme de $Ni_3(In_{0.53}Ga_{0.47})As$ permettant de diminuer la résistivité de contact jusqu'à $\rho_C = 5.6 \times 10^{-6}$ $\Omega.cm^2$. La métallisation de contact utilisée sur n-InP doit quant à elle être composée de Ni_2P, cette dernière donnant accès à une résistivité de contact de 4.3×10^{-6} $\Omega.cm^2$ après dépôt et de 7.3×10^{-6} $\Omega.cm^2$ après un traitement thermique conduit à 350 °C. Ces métallisations étant situées en fond de cavités, des plugs sont alors intégrés. Les cavités de contacts mesurant 40 µm x 500 µm sur InP et 5 µm x 500 µm sur InGaAs, de nouvelles cavités, plus petites, doivent être définies pour permettre la CMP damascène des plugs. De fait, une nouvelle encapsulation diélectrique composée de SiN et SiO_2 est réalisée et des cavités de quelques μm^2 sont ouvertes jusqu'à la métallisation de contact. Dès lors, une couche de nucléation servant également de barrière à la diffusion du F est déposée. Alors qu'elle est traditionnellement composée de Ti/TiN déposés par CVD, une solution innovante consiste à déposer du W dépourvu de F. Enfin, le métal de remplissage qui n'est autre que du W est déposé et une CMP damascène finale est conduite afin d'isoler électriquement les contacts les uns des autres.

CONTRIBUTIONS

FIRST AUTHOR PEER REVIEW PUBLICATION:

E. Ghegin, F. Nemouchi, J. Labar, C. Perrin, K. Hoummada, S. Favier, S. Gurban, and I. Sagnes. Phase formation in the Ni/InP contacts for heterogeneous III/V-Silicon photonic integration. *Microelectronic Engineering*, doi:10.1016/j.mee.2015.11.013, 2015.

CO-AUTHOR PEER REVIEW PUBLICATIONS:

Ph. Rodriguez, L. Toselli, **E. Ghegin**, N. Chevalier, N. Rochat, E. Martinez, and F. Nemouchi. In situ cleaning of InGaAs surfaces prior to low contact resistance metallization. *Microelectronic Engineering*, doi:10.1016/j.mee.2015.12.008, 2015.

Philippe Rodriguez, Laura Toselli, **Elodie Ghegin**, Mickaël Rebaud, Névine Rochat, Nicolas Chevalier, Eugénie Martinez, and Fabrice Nemouchi. Cleaning of InGaAs and InP layers for Nanoelectronics and Photonics contact technology applications. *ECS Transactions*, 69(8):251–259, 2015.

C. Perrin, **E. Ghegin**, S. Zhiou, F. Nemouchi, P. Rodriguez, P. Gergaud, P. Maugis, D. Mangelinck, and K. Hoummada. Formation of $Ni_3InGaAs$ phase in Ni/InGaAs contact at low temperature. *Applied Physics Letters*, 2019:131902, 2016.

INTERNATIONAL CONFERENCES:

Solid state reaction of Ni thin film on n-InP substrate for III-V laser contact technology, **E. Ghegin**, F. Nemouchi, J. Lábár, S. Favier, C. Perrin, K. Hoummada, S. Gurbán, P. Gergaud, IEEE 2015 International Interconnect Technology Conference / Materials for Advanced Metallization Conference (IITC/MAM 2015), May 18-21, 2015, Grenoble, France.

Elaboration of Ni/InP contacts: Solid state reactions and associated mechanisms, **E. Ghegin**, F. Nemouchi, J. Lábár, C. Perrin, K. Hoummada, S. Favier, S. Gurbán, I. Sagnes, 2015 International Workshop on Junction Technology (IWJT2015), June 11-12, 2015, Kyoto, Japan. **Best paper award of IWJT 2015.**

Towards contact integration for III-V/Silicon heterogeneous Photonics devices, **E. Ghegin**, Ph. Rodriguez, F. Nemouchi, Ch. Jany, M. Brihoum, B. Szelag, IITC/AMC, May 2016, San Jose, USA

Metallurgical Studies of Integrable Ni-based Contacts For Their Use in III-V/Si Heterogeneous Photonics Devices, **E. Ghegin**, F. Nemouchi, C. Perrin, K. Hoummada, J. Lábár, S. Zhiou, Ph. Rodriguez, I.Sagnes, C. Jany, Silicon Nanoelectronics Workshop (SNW), June, 2016, HI.

Reaction of Ni with p-InGaAs at 350°C RTP, Lábár J. L., Menyhárd M., Gurbán S., Hoummada K., **Ghegin E**., Nemouchi, IMC Conference, à Prague, September 7-12th 2014, Prague, Czech Republic.

Contacting n-InP with Ni, János L. Lábár, M. Menyhárd , S. Gurbán, A.A. Koós, F. Nemouchi, **E. Ghegin**, Exmatec 2014, June 18-20th 2014, Delphi, Greece.

In situ cleaning/passivation of surfaces for contact technology on III-V materials, Ph. Rodriguez, L. Toselli, **E. Ghegin**, F. Nemouchi, N. Rochat, E. Martinez, IEEE 2015 International Interconnect

Technology Conference / Materials for Advanced Metallization Conference (IITC/MAM 2015), May 18-21, 2015, Grenoble, France.

InGaAs Surface Pretreatment prior to Metal Solid-State Reactions for Low Resistance Contacts, Ph. Rodriguez, L. Toselli, **E. Ghegin**, N. Rochat, N. Chevalier, E. Martinez, F. Nemouchi, 2015 International Workshop on Junction Technology (IWJT2015), June 11-12, 2015, Kyoto, Japan.

Challenges of 3D VLSI-CoolCube™ process with p-Ge-OI and n-InGaAs-OI for Ultimate CMOS Nodes, F. Nemouchi, L. Hutin, H. Boutry, Ph. Rodriguez, **E. Ghegin**, J. Borrel, Y. Morand, S. Kerdiles, P. Batude, M. Vinet, Silicon Nanoelectronics Workshop 2015 (SNW2015), June 14-15, 2015, Kyoto, Japan.

Cleaning of InGaAs and InP Layers for Nanoelectronic and Photonic Contact Technology Applications, Ph. Rodriguez, L. Toselli, **E. Ghegin**, M. Rebaud, N. Rochat, N. Chevalier, E. Martinez, F. Nemouchi, 228th ECS Meeting, October 11-16, 2015, Phoenix, USA.

High Performance CMOS FDSOI Devices activated at Low Temperature, L. Pasini, P. Batude, J. Lacord, M. Casse, B. Mathieu, B. Sklenard, F. Piegas Luce, J. Micout, F. Mazen, P. Besson, **E. Ghegin**, J. Borrel, R. Daubriac, L. Hutin, D. Blachier, D. Barge, S. Chhun, A. Cros, G. Ghibaudo, J-P. Barnes, N. Rambal, V. Lapras, J. Mazurier, O. Weber, F. Andrieu, C. Fenouillet-Beranger, Q. Rafhay, F. Cristiano, M. Haond, F. Boeuf and M. Vinet, VLSI Technology and circuits 2016, Honolulu, HI.

PATENTS

Intégration de contacts sur III-V compatibles avec une filière silicium, GHEGIN Elodie - NEMOUCHI Fabrice - RODRIGUEZ Philippe - JANY Christophe - SZELAG Bertrand.

Formation de contacts ohmiques pour un dispositif doté d'une région en matériau III-V et d'une région en un autre matériau semi-conducteur, RODRIGUEZ Philippe - GHEGIN Elodie -NEMOUCHI Fabrice.

Report collectif de puces contenant un empilement III/V laser sur substrat SOI partternée, NEMOUCHI Fabrice - GHEGIN Elodie - RODRIGUEZ Philippe - BAUDOT Charles.